User Manual

SXC-ARL30 V2.0



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SXC-ARL30 Product User Manual

(Version 2.0)

Version:		
NO.	Description	Issue Date:
V2.0	1. Replaced the DDR5 SO-DIMM socket with onboard dual-channel LPDDR5-6400 memory, available in 8 GB, 16 GB, and 32 GB configurations. 2. Added two M.2 Key M slots (M.2_N2 and M.2_N3, as labeled on the motherboard), supporting M.2 2280 NVMe SSDs. 3. Upgraded the power input design from 19 V/20 V DC to a wide input range of 9–36 V DC. 4. Revised the power connector configuration: the DC connector is included as standard, and the Phoenix terminal block is available as an option. 5. Added GPIO support.	2026/04/07
V1.0	Initial Version (EN)	2024/10/25

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Warning

1. Before using the product, carefully read the manual to ensure proper installation and operation.
2. If you are not ready to install any extension card, store it in an anti-static protective bag to prevent damage.
3. To discharge any static electricity, briefly touch a grounded metal object before removing the extension card from the protective bag.
4. Always wear anti-static gloves and handle the card by its edges to avoid damaging sensitive components.
5. Verify that the power supply voltage is correct before connecting the motherboard to the power supply.
6. To prevent electric shock or damage, always turn off the AC power or unplug the power cord before removing or reconfiguring the motherboard or any components.
7. Unplug the AC power cord from the outlet before relocating the motherboard or any components.
8. Ensure all power cords are unplugged before connecting or disconnecting any equipment to avoid electrical hazards.
9. Wait at least 30 seconds after powering off the system before powering it on again to prevent unnecessary wear.
10. If any issues arise during operation, consult a qualified professional for assistance.
11. This product may cause radio interference in certain environments; if necessary, users should take appropriate measures to mitigate such interference.

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Chapter 1 Product Introduction

1.1 Brief Introduction

The SXC-ARL30 is an embedded PC powered by the Intel Meteor Lake/Arrow Lake-U/H platform. It offers high computing performance with a choice of passive or active cooling solutions, ideal for industrial and commercial applications.

1.2 Parameters

Processor: Intel Meteor Lake/Arrow Lake-U/H Series

CPU	Cores/Threads	Max Turbo Frequency	Base Frequency	Cache	TDP
Intel® Core™ Ultra 5 125U	12C(2P+8E+2LP-E)/14T	4.3GHz P-Core:4.3GHz E-Core:3.6GHz LP E-Core:2.1GHz	1.3GHz P-Core:1.3GHz E-Core:800MHz LP E-Core:700MHz	12MB	15W (Max Turbo Power: 57W) Default PL1/PL2: 15W
Intel® Core™ Ultra 5 225U	12C(2P+8E+2LP-E)/14T	4.8GHz P-Core:4.8GHz E-Core:3.8GHz LP E-Core:2.4GHz	1.5GHz P-Core:1.5GHz E-Core:1.3GHz LP E-Core:700MHz	12MB	15W (Max Turbo Power: 57W) Default PL1/PL2: 15W
Intel® Core™ Ultra 5 125H	14C(4P+8E+2LP-E)/18T	4.5GHz P-Core:4.5GHz E-Core:3.6GHz LP E-Core:2.5GHz	1.2GHz P-Core:1.2GHz E-Core:700MHz LP E-Core:700MHz	18MB	28W (Max Turbo Power: 115W) Default PL1/PL2: 28W

GPU: **Integrated Intel Graphics/Intel® Arc™ graphics**

CPU	GPU Name	Max Dynamic Frequency	GPU Peak TOPS (Int8)	X^e-cores
Intel® Core™ Ultra 5 125U	Intel® Graphics	1.85 GHz	7	4
Intel® Core™ Ultra 5 225U	Intel® Graphics	2.00GHz	8	4
Intel® Core™ Ultra 5 125H	Intel® Arc™ graphics	2.20 GHz	18	7

Display Interfaces: 4 × HDMI 2.0b ports with HDCP 2.3 support (labeled onboard: HDMI12 / HDMI34), 1 x USB-C Type-C port (DP 1.4 supported).

NPU: **Intel® AI Boost**

CPU	NPU Name	NPU Peak TOPS (Int8)	AI Software Frameworks Supported by NPU
Intel® Core™ Ultra 5 125U	Intel® AI Boost	11	OpenVINO™, WindowsML, DirectML, ONNX RT
Intel® Core™ Ultra 5 225U	Intel® AI Boost	12	OpenVINO™, WindowsML, DirectML, ONNX RT
Intel® Core™ Ultra 5 125H	Intel® AI Boost	11	OpenVINO™, WindowsML, DirectML, ONNX RT

Memory: Onboard dual-channel LPDDR5 memory, 6400 MT/s; 8 GB/16 GB/32 GB

Storage:

- 3 x M.2 Key M slots for 2280 NVMe SSDs (labeled M.2_N1/N2/N3 onboard)
- 1 x M.2 Key B slot for a 2242/2280 SATA SSD or 3042 4G module (labeled M.2_SW onboard)

Expansion: 1 x M.2 Key E slot for 2230 Wi-Fi and Bluetooth modules, support PCIE/USB2.0/CNVi. (labeled M.2_E onboard)

Nano SIM: 1x Nano SIM Slot. The slot supports Nano SIM and enables 4G communication when used with a compatible M.2_4G module.

Audio: SenaryTech SN6186 High-Definition Audio Codec, 1 x Line-out, 1 x Mic-in.

Ethernet: 2 × RJ45 Ethernet ports for high-speed network connectivity

- 1 × Intel® I219 – Data rate per port: 1.0 GbE
- 1 × Intel® I226 – Data rate per port: 2.5 GbE

USB Interfaces:

- 4 × USB 3.2 Gen 2 Type-A ports (up to 10 Gbps) (labeled USB30/USB31 onboard)
- 2 × USB 2.0 Type-A ports (up to 480 Mbps) (labeled USB20/USB21 onboard)
- 1 × USB Type-C port
  - Supports USB 3.2 Gen 2 (up to 10 Gbps)
  - Supports DisplayPort 1.4 (DP 1.4)

Serial I/O (COM Ports): 2 x COM DB9 interfaces, with RS232 configuration by default and RS485 optional.

GPIO: 8-bit GPIO, optional with COM2 (2.0mm pitch, labeled GPIO onboard)

TPM: Optional external TPM module support (Infineon SLB9670).

Other Internal Connectors:

- 1 x JAT hardware auto power-on header, 2.0 mm pitch (labeled JAT onboard)
- 1 x MCU battery connector (labeled JBAT_MCU onboard)
- 1 x MCU connector (labeled JMCU onboard)
- 1 x RTC battery connector (labeled JBAT onboard)
- 1 x Nano-SIM card slot (labeled SIM onboard)
- 1 x 5V, 4-pin CPU fan header, 1.25 mm pitch (labeled CPUFAN onboard)
- 1 x 5V, 4-pin system fan header, 1.25 mm pitch (labeled SYSFAN onboard; optional)
- 1 x Clear CMOS header, 2.0 mm pitch (labeled CLR_CMOS onboard)
- 1 x 4-pin wired power switch header, 1.5 mm pitch (labeled FP_OUT onboard)

MCU Timer: Equipped with a MCU Timer, allowing users to schedule independent power on/off

times for each day of the week.

Wired Control: 1 x Wired Control Remote Switch (PH1.5mm 4PIN)

Power: 9V-36V DC-IN (5.5x2.5mm), Phoenix_2PIN optional(3.81mm)

Board Dimension: 177.5mm x 132mm

Chassis Dimension: 190mm x 150mm x35mm (L x W x H)

Cooling Method:

- Passive: Intel Meteor Lake/Arrow Lake-U Series Processors
- Active: Intel Meteor Lake/Arrow Lake-H Series Processors

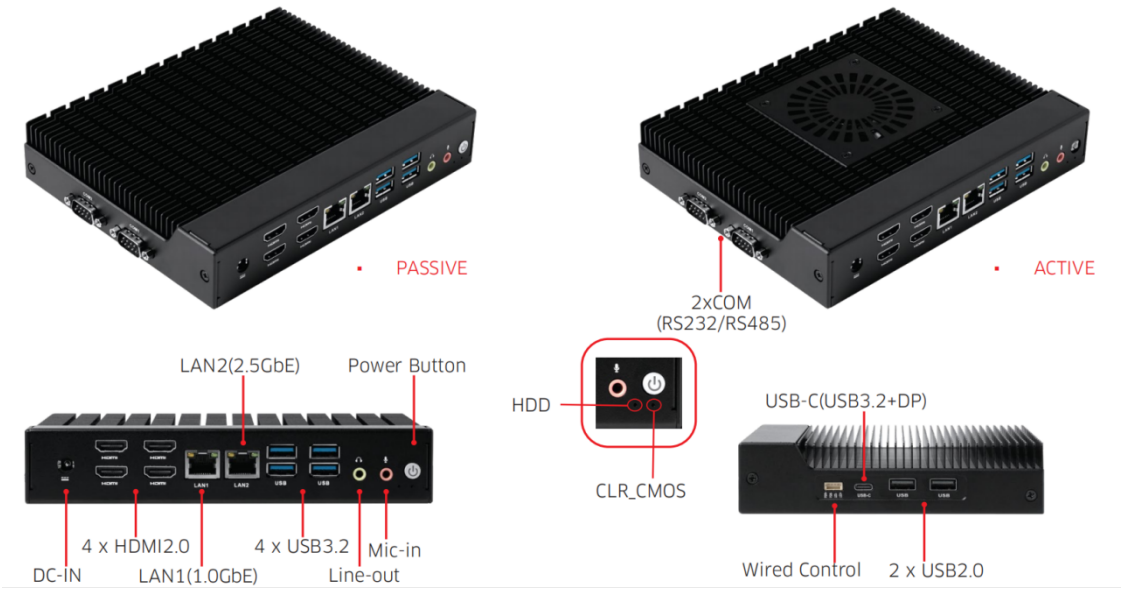
Operating Temperature: -20℃~60℃

Storage Temperature: -40℃~80℃

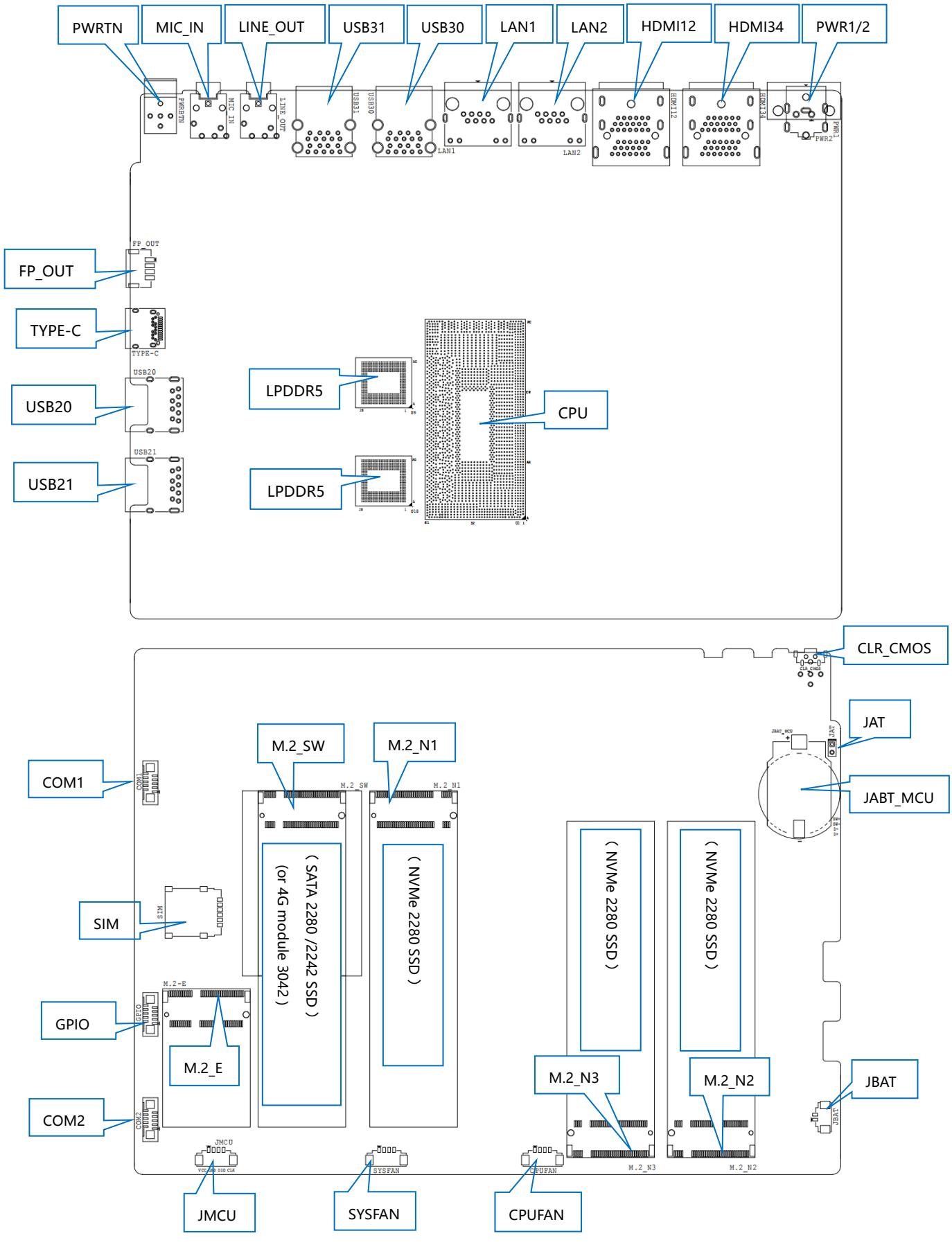
OS Support: Supports Windows 11 version 24H2, Ubuntu 24.04, and other operating systems released in or after 2024. Note: Windows 10 and earlier versions of Ubuntu are not supported. For Windows processor compatibility, refer to the Microsoft Windows 11 24H2 Supported Intel Processors list.

1.3 Product Overview

I/O Interfaces



1.4 Connector Diagram



Chapter 2 Hardware

2.1 Installations

Please refer to the following steps for installation:

1. Read the user manual carefully to make sure all the adjustments on the SXC-ARL30 are correct.
2. Installing the Memory:
   - Press the ejector tab of the memory slot outwards with your fingertips.
   - Hold the memory module and align the key to the module with that on the memory slot.
   - Gently push the module into the slot until the ejector levers return completely to the closed position, holding the module in place when the module touches the bottom of the slot. To remove the module, press the ejector levers outwards to unseat the module.
3. Installing the expansion cards:
   - Locate the expansion slots and remove the screw, insert the cards into the slot at a 45-degree angle then attach the screw to the expansion cards, gently press down on it then install the screw back.
4. Connect all signal wires, cables, panel control wiring, and power supplies.
5. Start the computer and complete the setup of the BIOS program.

The board's components are integrated circuits and can easily be damaged by Electrostatic Discharge or ESD; therefore, please follow the instructions:

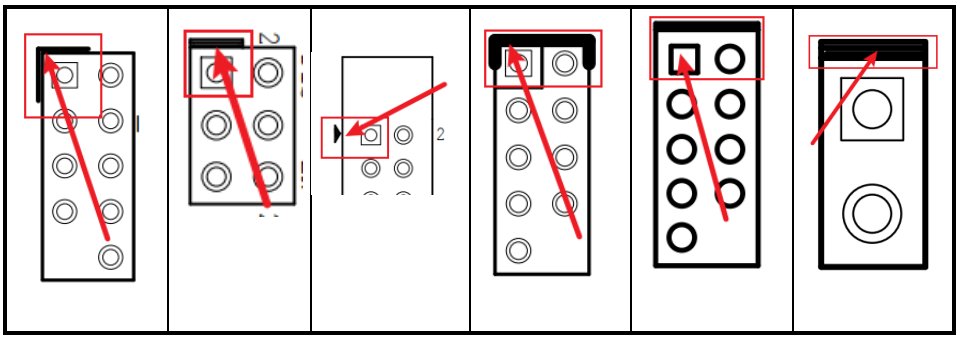
- Hold the board's edge when handing, and do not touch onboard pins, components, or plug sockets.
- When touching integrated circuit components (such as CPU, RAM, etc.), please wear an anti-static wrist strap/glove to avoid electrostatic discharge damage to the board or other sensitive components.
- Before installing the integrated circuits/sensitive components, place the sensitive components in anti-static bags to keep them safe from ESD.
- Please make sure the power switch is OFF before plugging the power plug.

2.2 Jumper Setting

Please configure the jumpers according to your requirements before installing the hardware.

How to identify the first header of jumpers and pins: Observe the mark beside the jumper or pins and find the header marked by “1” or bold line or triangular symbol. Or observe the rear panel and the header with a square solder pad is the first header.

Illustration:



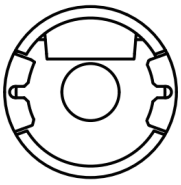
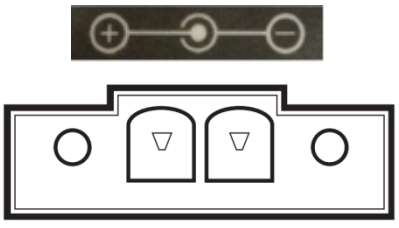
2.3 Memory

The system features onboard dual-channel LPDDR5 memory, available in **8 GB**, **16 GB**, or **32 GB** configurations. **Please Note:** The onboard LPDDR5 memory is factory-installed and is **not user-upgradable**.

2.4 Power Input (Labeled PWR1 / PWR2 onboard)

The system supports a 9–36 V DC power input through either of the following connectors:

- PWR1: DC power jack (5.5 × 2.5 mm). A 19 V DC power adapter is available as an option.
- PWR2: 2-pin Phoenix terminal block (3.81 mm pitch) (optional).

PWR1: DC-IN Jack (5.5x2.5mm)	PWR2: Phoenix Connector (2PIN) (3.81mm pitch)
	

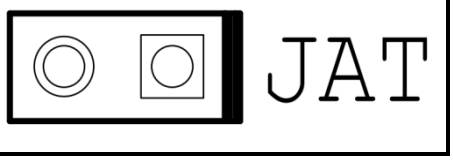
2.5 Hardware Auto Power-On (Labeled JAT onboard)

The **JAT** header (labeled **JAT** onboard) controls the hardware power-on auto-start function.

Install the appropriate jumper to enable or disable this feature.

JAT Settings:

Enable	Disable
1-2	NC

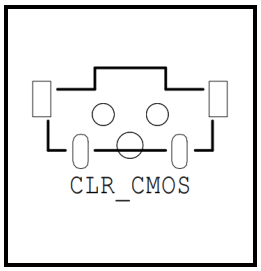


2.6 CMOS Clearance/Retention (Labeled CLR_CMOS onboard)

The CLR_CMOS button (labeled onboard: CLR_CMOS) provides two functions depending on the system power state. When the system is powered off, the CLR_CMOS button functions as a Clear CMOS button. When the system is powered on, the same button functions as a Reset button to restart the system.

The CMOS memory is powered by the onboard coin-cell battery. Clearing the CMOS restores all BIOS settings to their factory defaults.

Clear CMOS (Labeled onboard: CLR_CMOS)



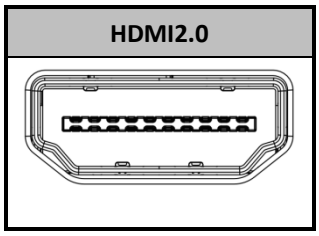
Steps to clear the CMOS:

1. Shut down the system and disconnect the power supply.
2. Press and hold the CLR_CMOS button for at least 3 seconds.
3. Reconnect the power supply and power on the system.
4. Press <Del> during startup to enter the BIOS Setup, then load the optimized default settings if required.

Do not clear the CMOS while the system is powered on, as this may damage the motherboard.

2.7 Display Interfaces

The system provides four HDMI 2.0 ports, supporting up to four simultaneous 4K @ 60 Hz displays. The system also supports the HDMI HPD Lock function.



HDMI HPD Lock

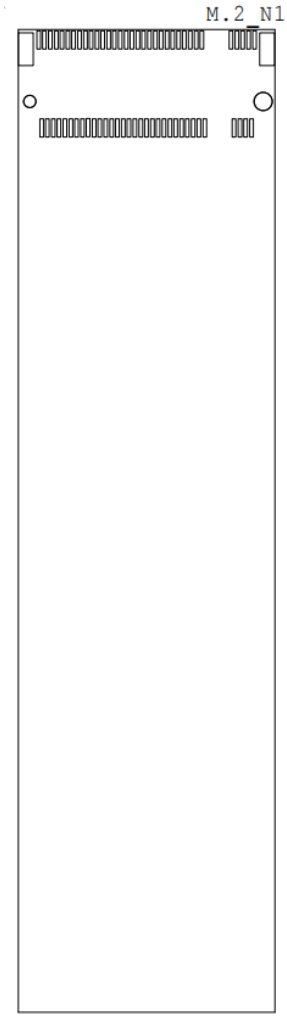
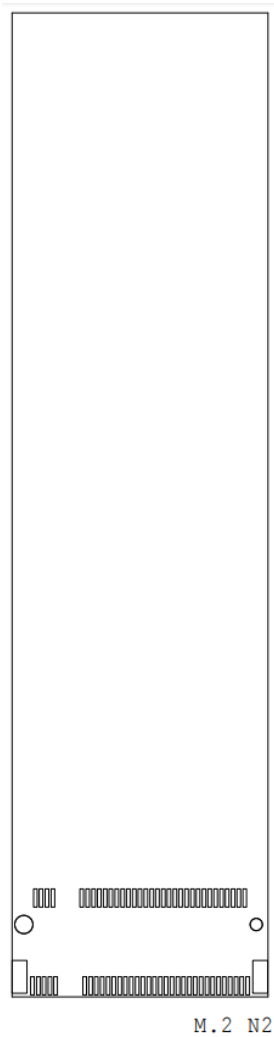
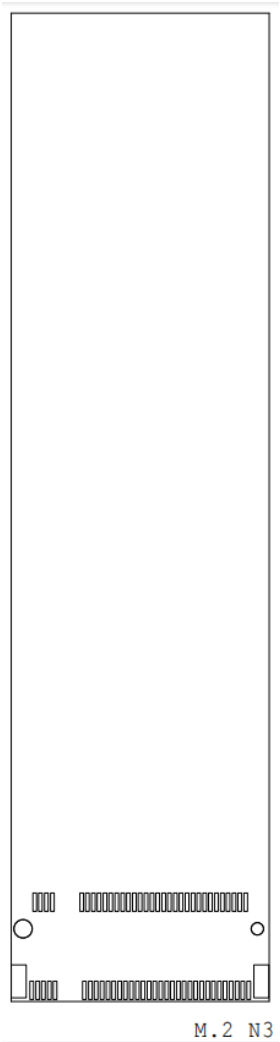
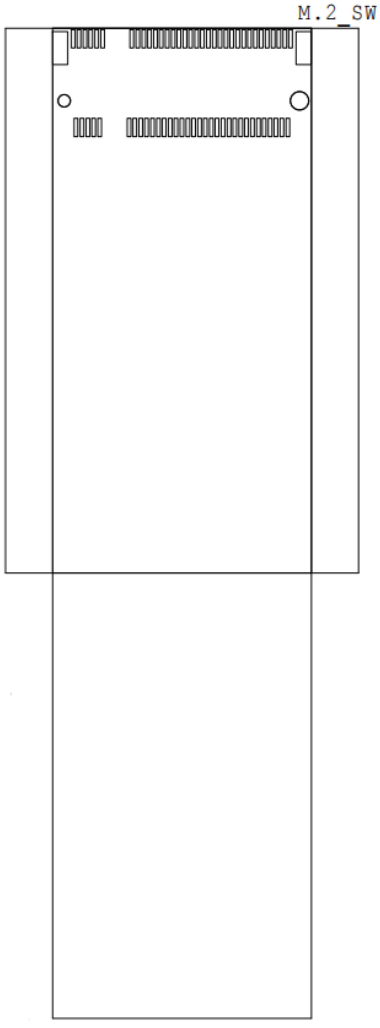
HDMI HPD Lock is designed for multi-display applications. When enabled in the BIOS, it locks the display connection status to help maintain the current display configuration.

The feature is recommended when multiple displays are configured as a video wall or extended display. If an HDMI cable is accidentally disconnected, **HDMI HPD Lock** prevents the operating system from detecting a display removal, helping to maintain the existing display layout.

2.8 Storage Interfaces (Labeled M.2_N1/N2/N3/M.2_SW onboard)

The system provides multiple M.2 storage and expansion interfaces, supporting NVMe SSDs, SATA SSDs, optional 4G modules.

- 3 x M.2 Key M slots for 2280 NVMe SSDs (labeled M.2_N1/N2/N3 onboard)
- 1 x M.2 Key B slot for a 2242/2280 SATA SSD or 3042 4G module (labeled M.2_SW onboard)

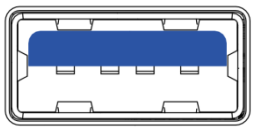
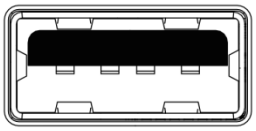
M.2_N1	M.2_N2	M.2_N3	M.2_SW
			

2.9 USB Interfaces (Labeled USB31/USB30/USB21/USB20/ TYPE-C onboard)

The system provides the following USB interfaces:

- **4 × USB 3.2 Gen 2 Type-A ports** (10 Gbps). *(Labeled onboard: **USB31/USB30**)*
- **2 × USB 2.0 Type-A ports** (480 Mbps). *(Labeled onboard: **USB20/USB21**)*
- **1 × USB 3.2 Gen 2 Type-C port** (10 Gbps). *(Labeled onboard: **TYPE-C**)*

USB Illustrations:

USB31/USB30	USB20/USB21	TYPE-C
		

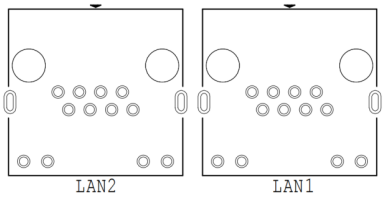
USB Wake-Up Function

The **USB 2.0 Type-A ports** located on the rear I/O panel *(labeled onboard: **USB20/USB21**)* provide **5V standby power (5VSB)**.These ports support **USB keyboard and mouse wake-up**, allowing the system to be powered on from **Sleep** or **Soft-Off (S5)** states, if AC power remains connected. The USB20 ports can also supply power to external USB devices with an output of **5V/0.5A**.

Note: The USB wake-up function is available only when the system remains connected to AC power. It is not supported when the system is completely disconnected from the power source.

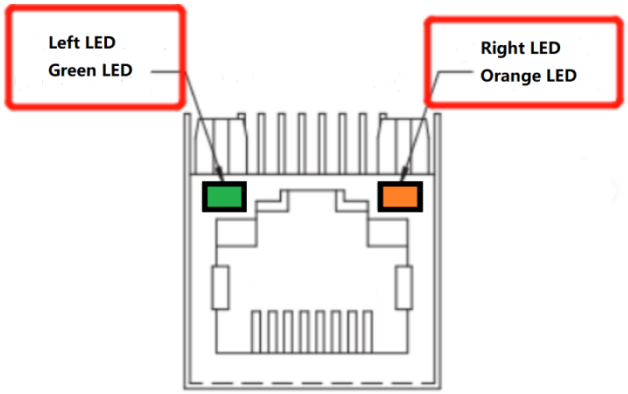
2.10 LAN (Labeled LAN1/LAN2 onboard)

The system provides two RJ45 Ethernet ports, LAN1 powered by an Intel® i219 1.0Gigabit Ethernet controller, supporting data rates of 10/100/1000Mbps. LAN2 powered by an Intel® i226 2.5Gigabit Ethernet controller, supporting data rates of 10/100/1000/2500Mbps. Both support Wake-on-LAN (WoL) via Magic Packet. Only LAN1 supports UEFI PXE Boot. To enable UEFI PXE Boot, enter the BIOS and configure: Advanced → Network Stack Configuration → IPv4 PXE Support → Enabled

LAN1/LAN2


Ethernet LED Indicators:

LILED (Green)	Function	ACTLED (Orange)	Function
On	Link Established	Blinking	Network Activity

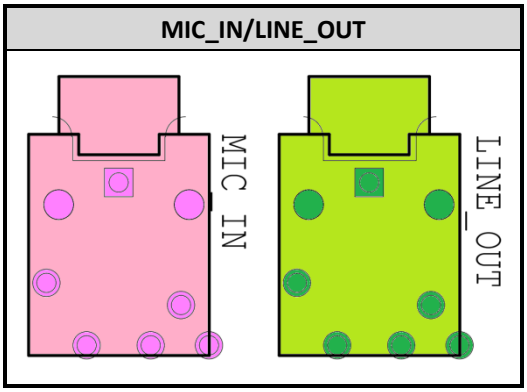


2.11 Audio Interfaces (Labeled MIC_IN / LINE_OUT onboard)

The system features a SenaryTech SN6186 High-Definition Audio codec and provides one set of 3.5 mm rear audio jacks.

- MIC_IN (Pink): Microphone input
- LINE_OUT (Green): Audio output

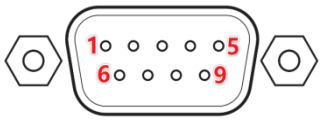
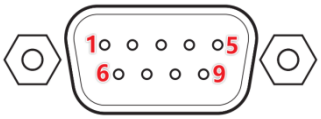
MIC_IN/LINE_OUT:



2.12 Serial Ports (Labeled COM1 / COM2 onboard)

The system provides two DB9 serial ports, supporting RS-232 by default. RS-485 is available as an optional choice through hardware modification.

COM1/COM2 (Labeled onboard: COM1, COM2)

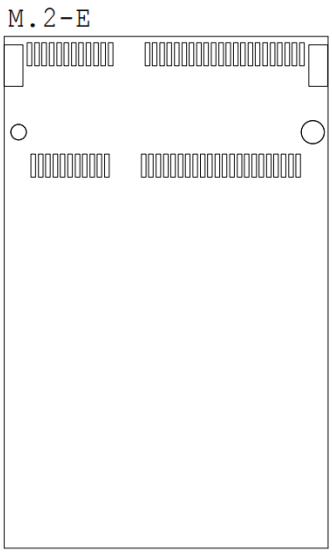
	**Default RS232 Mode**					
	Pin	1	2	3	4	5
	Signal	DCD#	RXD	TXD	DTR#	GND
	Pin	6	7	8	9	
	Signal	DSR#	RTS#	CTS#	RI#	
	**Optional RS485 Mode**					
	Pin	1	2	3	4	5
	Signal	DATA-	DATA+	(NC)	(NC)	(NC)
	Pin	6	7	8	9	
	Signal	(NC)	(NC)	(NC)	(NC)	

2.13 Expansion Slots (Labeled M.2_E onboard)

The system provides a M.2 key E interfaces for wireless expansion.

- 1 x M.2 Key E slot for 2230 WiFi&BT Module, PCIE& CNVi/USB2.0 signal (labeled M.2_E onboard)

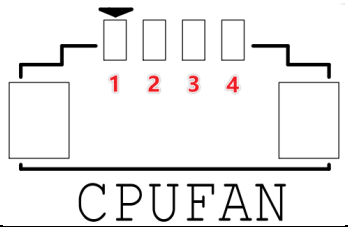
M.2-E



2.14 CPU Fan/System Fan (Labeled as CPUFAN, SYSFAN onboard)

The system provides a 5 V 4-pin CPU fan header (1.25 mm pitch) (Labeled CPUFAN onboard), a 5 V 4-pin system fan header optional (1.25 mm pitch) (Labeled SYSFAN onboard).

CPU FAN PIN Definition (Labeled CPUFAN onboard)

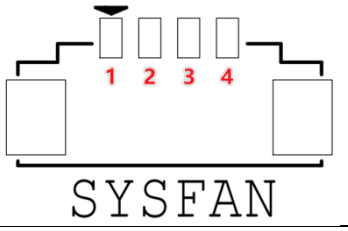


	SYSFAN		CPUFAN	
VGTC	RF7	RF8	RF3	RF4
GVTC	RF5	RF6	RF1	RF2

Default RF3 and RF4 Populated				
Pin	1	2	3	4
Signal	5V	GND	TAC	CTL

Optional RF1 and RF2 Populated				
Pin	1	2	3	4
Signal	GND	5V	TAC	CTL

SYSTEM FAN PIN Definition (Labeled SYSFAN onboard) (Optional)



	SYSFAN		CPUFAN	
VGTC	RF7	RF8	RF3	RF4
GVTC	RF5	RF6	RF1	RF2

Default RF7 and RF8 Populated				
Pin	1	2	3	4
Signal	5V	GND	TAC	CTL

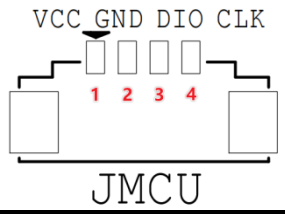
Optional RF5 and RF6 Populated				
Pin	1	2	3	4
Signal	GND	5V	TAC	CTL

2.15 MCU Timer (Labeled JMCU onboard)

The system integrates an MCU timer that supports scheduled power-on and power-off operations. Independent schedules can be configured for each day of the week in the BIOS Setup Utility.

JMCU Programming Header (Labeled JMCU Onboard)

The JMCU header is reserved for MCU firmware programming.

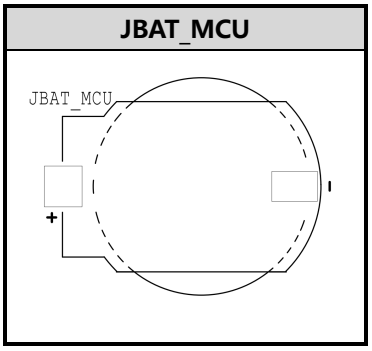


Pin	1	2	3	4
Signal	VCC	GND	DIO	CLK

***Caution: Do not reprogram the MCU firmware unless instructed by MAXTANG technical support. Improper firmware programming may result in system malfunction or motherboard damage.

Installing a CR2032 coin-cell battery on the JBAT_MCU header enables the timer function, allowing the system to automatically power on and power off according to independently configured schedules for each day of the week.

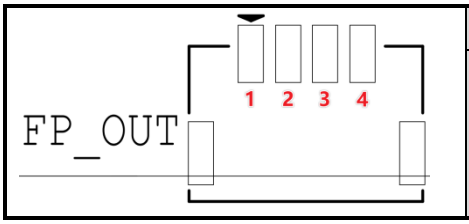
JBAT_MCU:



2.16 Remote Control Switch (Labeled FP_OUT onboard)

The system's board integrates a remote-control switch interface, allowing users to power the system on or off through an external switch.

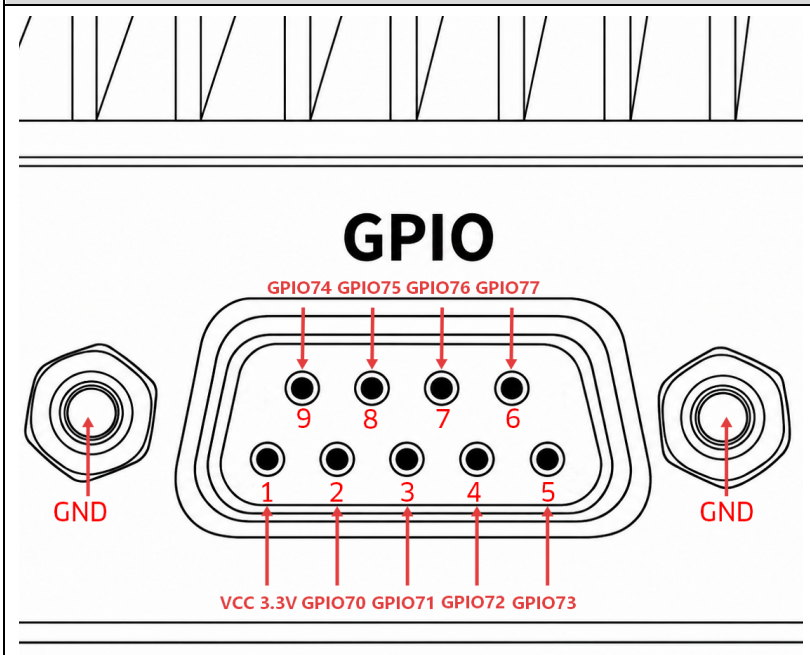
FP_OUT Pin Definition (Labeled: FP_OUT Onboard) (PH1.5mm 4PIN)



Pin	1	2	3	4
Signal	SW+	SW-	D-	D+

2.17 GPIO Optional (Labeled GPIO onboard)

The system's side-panel DB9 connector supports COM2 by default and can be configured as a GPIO interface as an optional hardware feature. The GPIO interface provides 8 programmable General-Purpose Input/Output (GPIO) signals for external device control and monitoring.

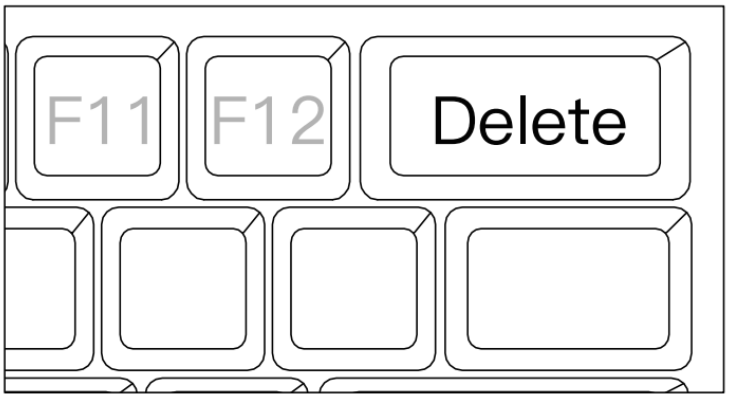
GPIO DB9 Connector	Mark	Pin	Signal
	1	VCC	3.3V
	2	IO0	GPIO70
	3	IO1	GPIO71
	4	IO2	GPIO72
	5	IO3	GPIO73
	6	IO4	GPIO74
	7	IO5	GPIO75
	8	IO6	GPIO76
	9	IO7	GPIO77

Note: The GPIO interface is available only on systems ordered with the optional GPIO configuration. When configured as GPIO, the connector cannot be used as the COM2 serial port.

Chapter 3 BIOS Setup

3.1 Entering the BIOS

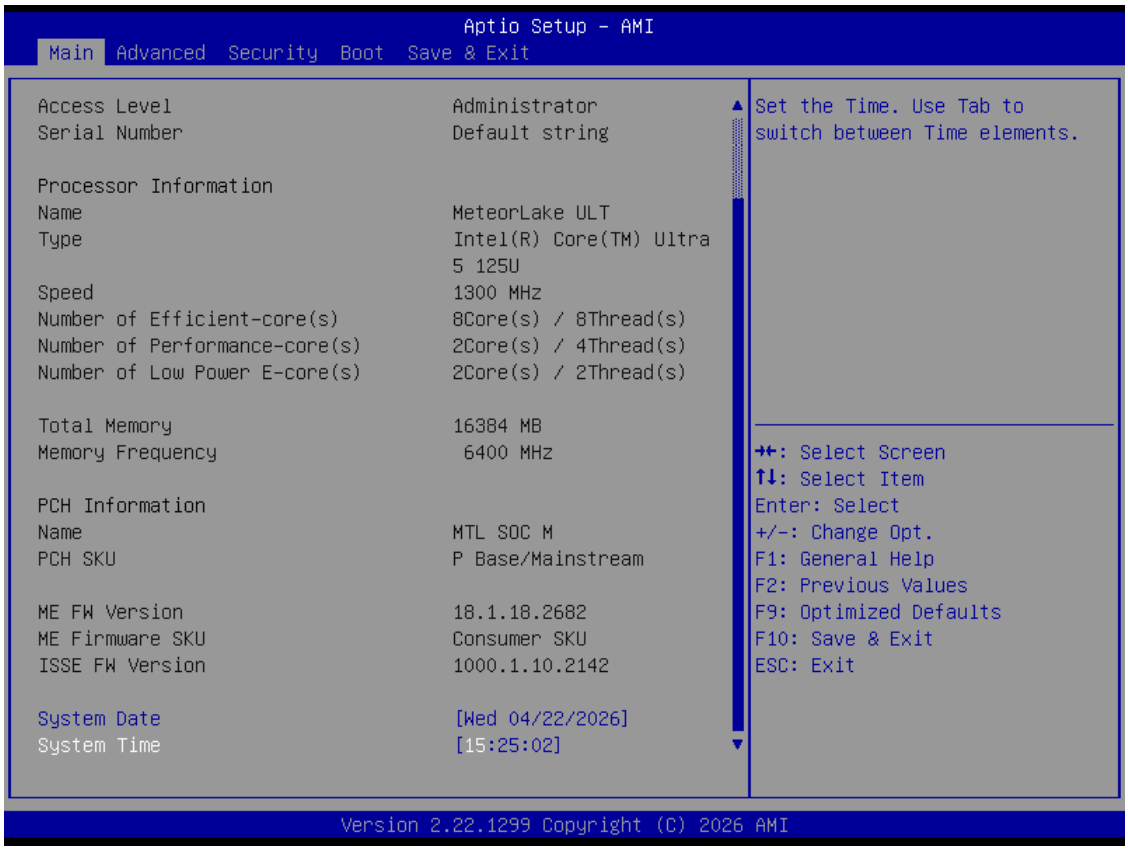
Entering BIOS Setup: Press the <Delete> key repeatedly during system startup to enter the BIOS Setup Utility.



BIOS Hot Keys:

Key	Function	Description
→ ←	Select Screen	Navigate between menu screens.
↑↓	Select Item	Move between menu items or options.
Enter	Select	Open a submenu or confirm a selection.
+/-	Change Option	Adjust values or change settings.
F1	General Help	Displays helpful information for the selected item.
F2	Previous Values	Load the previously saved settings.
F9	Optimized Defaults	Restore factory default settings.
F10	Save & Exit	Save changes and exit BIOS.
ESC	Exit	Exit BIOS or return to the previous menu.

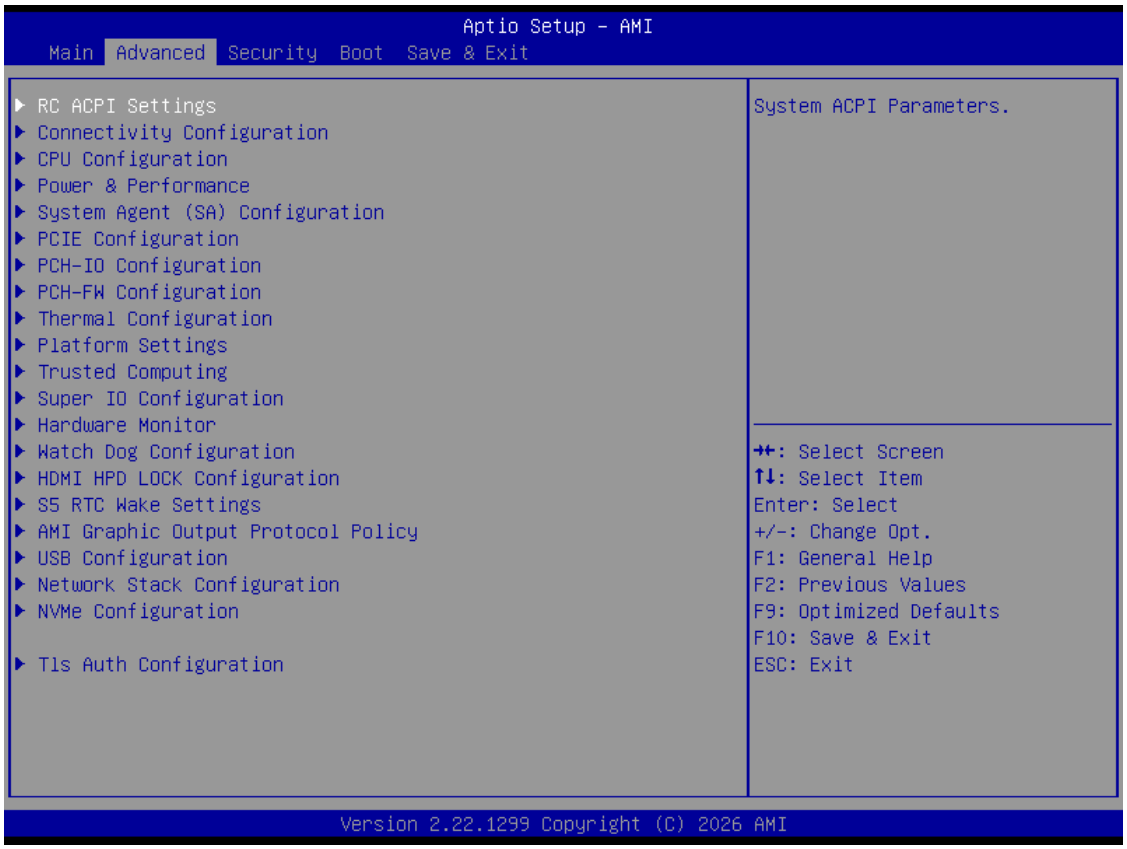
3.2 Main Menu (BIOS Info, Date, Time)



The Main menu displays basic system information and allows you to configure the system date and time.

- **BIOS Information** – Displays BIOS version and firmware information.
- **BIOS Vendor** – Displays the BIOS vendor (American Megatrends).
- **BIOS Version** – Displays the installed BIOS version.
- **Build Date and Time** – Displays the BIOS build date and time.
- **Processor Information** – Displays the installed processor information.
- **Total Memory** – Displays the total installed system memory.
- **Memory Frequency** – Displays the current memory operating frequency.
- **PCH Information** – Displays Platform Controller Hub (PCH) information.
- **PCH SKU** – Displays the PCH model.
- **ME FW Version** – Displays the Intel® Management Engine firmware version.
- **System Date** – Sets the system date in MM/DD/YYYY format.
- **System Time** – Sets the system time in HH:MM:SS format.

3.3 Advanced Setting

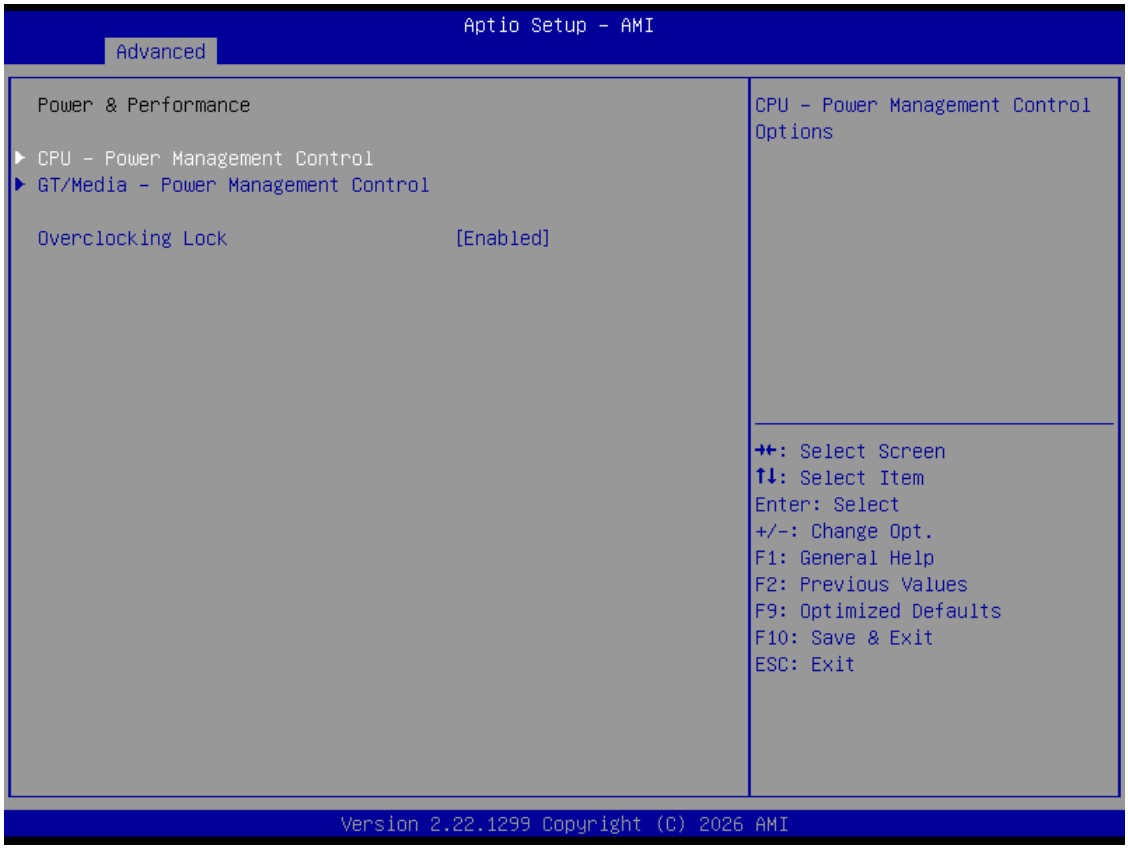


The **Advanced** menu provides access to advanced system configuration options, including processor, chipset, power management, onboard devices, security, and peripheral settings.

- **RC ACPI Settings**:Configures ACPI power management and related system settings.
- **Connectivity Configuration**:Configures system connectivity and related device settings.
- **CPU Configuration**:Displays processor information and configures CPU-related features.
- **Power & Performance**:Configures system power management and performance-related settings.
- **System Agent (SA) Configuration**:Configures System Agent settings, including graphics, memory, and related system functions.
- **PCIE Configuration**:Configures PCI Express (PCIe) devices and related features.
- **PCH-IO Configuration**:Configures Platform Controller Hub (PCH) I/O functions and related device settings.
- **PCH-FW Configuration**:Configures Platform Controller Hub (PCH) firmware-related settings.
- **Thermal Configuration**:Configures system thermal management settings.
- **Platform Settings**:Configures platform-specific system settings.
- **Trusted Computing**:Configures Trusted Platform Module (TPM) and related security features.
- **Super IO Configuration**:Configures Super I/O devices and related functions.
- **Hardware Monitor**:Displays system hardware monitoring information, such as temperatures, voltages, and fan status.
- **Watch Dog Configuration**:Configures the system watchdog timer.
- **HDMI HPD LOCK Configuration**:Configures the HDMI Hot Plug Detect (HPD) lock function.

- **S5 RTC Wake Settings**:Configures RTC-based system wake-up from the S5 (Soft Off) state.
- **AMI Graphic Output Protocol Policy**: Configures the AMI Graphics Output Protocol (GOP) policy.
- **USB Configuration**: Configures USB controllers, ports, and related features.
- **Network Stack Configuration**: Configures the UEFI network stack and related network boot features.
- **NVMe Configuration**:Displays and configures NVMe devices and related information.
- **Tls Auth Configuration**:Configures TLS authentication settings.

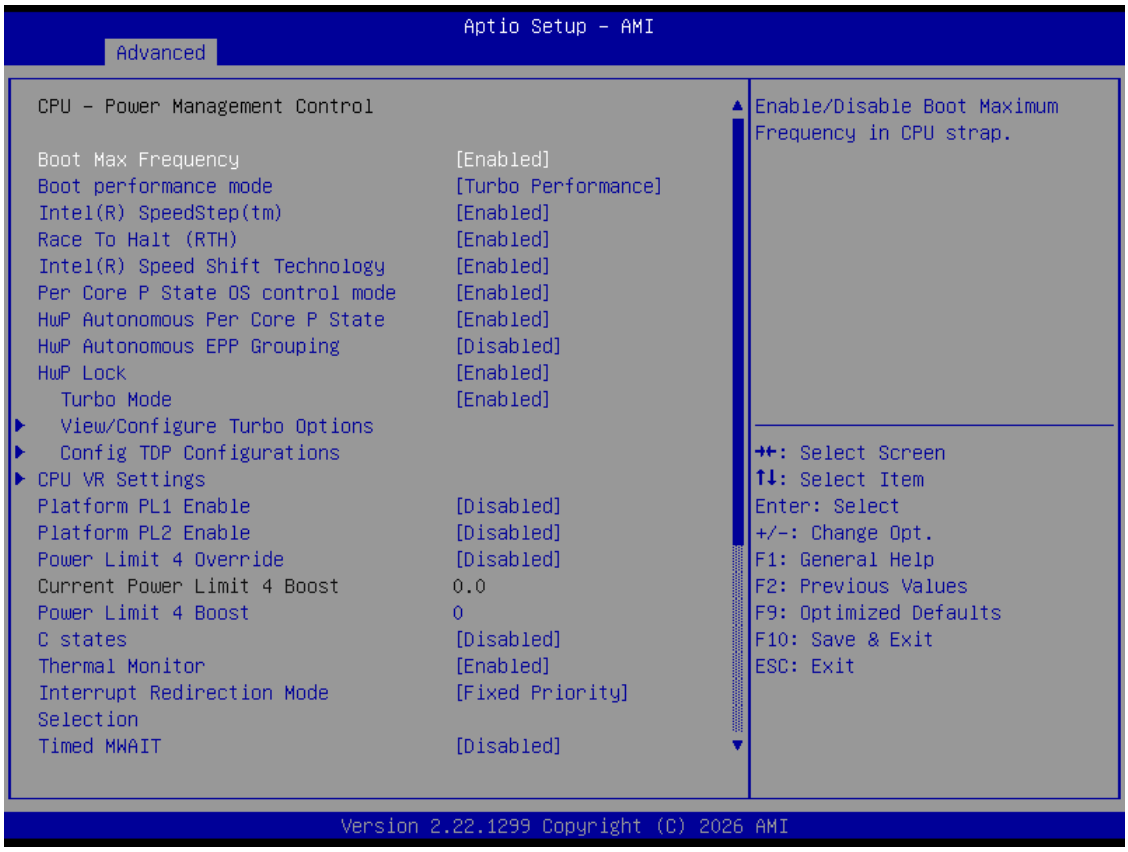
3.3.1 Power & Performance



The Power & Performance menu provides advanced processor power management and graphics power configuration options. The following submenus are available:

- **CPU-Power Management Control** – Configures processor power management settings.
- **GT/Media-Power Management Control** – Configures integrated graphics (GT) power management settings.

3.3.2 CPU-Power Management Control



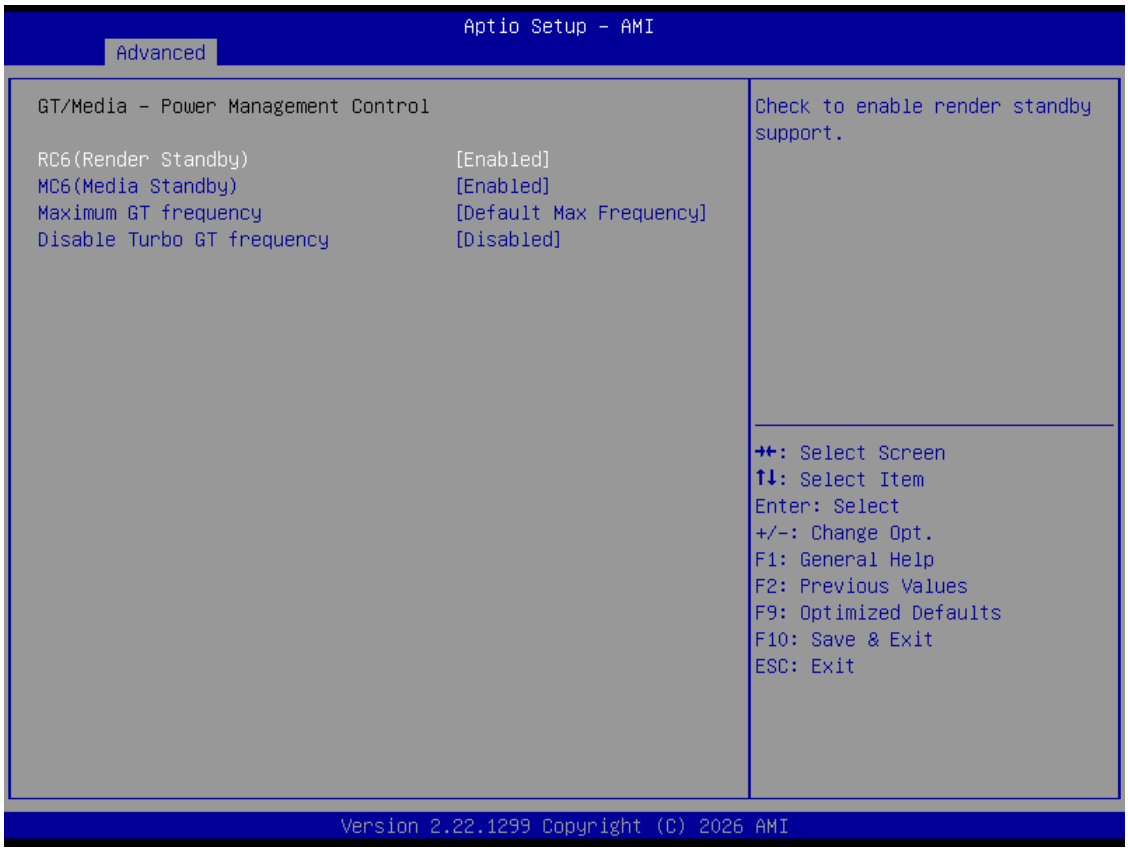
The CPU-Power Management Control menu provides processor power management and performance-related settings.

- **Boot Max Frequency:** Boot Max Frequency, default enabled.
- **Boot Performance Mode:** Selects the processor performance mode during system boot. The default setting is Turbo Performance. Available options include Max Battery, Max Non-Turbo Performance, and Turbo Performance.
- **Intel® SpeedStep™:** Enables dynamic adjustment of the processor operating frequency and voltage to optimize system performance while reducing power consumption.
- **Intel® Speed Shift Technology:** Enables Hardware-Controlled Performance (HWP), allowing the processor to dynamically adjust its operating frequency based on workload demand and system conditions for improved responsiveness and power efficiency. Enabled by default.
- **Per Core P-State OS Control Mode:** Allows the operating system to manage the performance state (P-State) of each processor core independently.
- **HWP Autonomous Per Core P-State:** Enables autonomous Hardware-Controlled Performance (HWP) management for each processor core.
- **HWP Autonomous EPP Grouping:** Configures Energy Performance Preference (EPP) grouping for Hardware-Controlled Performance (HWP).
- **Turbo Mode:** The Turbo mode refers to Nehalem's "Integrated Power Gate" power

management technology, which allows running off some cores and adding power to the others so that they run at a higher frequency. The capacity of the entire CPU remains unchanged, and the efficiency of the CPU is optimized. Default Enabled.

- **EPB Override over PCIe:** Allows the Energy Performance Bias (EPB) setting to override PCIe power management behavior.
- **Platform PL1 Enable:** Enables Platform Power Limit 1 (PL1). Disabled by default.
- **Platform PL2 Enable:** Enables Platform Power Limit 2 (PL2). Disabled by default.
- **Power Limit 4 Override:** Enables manual override of Platform Power Limit 4 (PL4). Disabled by default.
- **C-States:** Enables processor idle power-saving states. Higher C-State levels place the processor into progressively deeper idle states, reducing power consumption while increasing wake-up latency. Enabled by default.
- **Enhanced C-States:** Enables enhanced processor idle power-saving features to further optimize power consumption during periods of low system activity. Enabled by default.

3.3.3 GT-Power Management Control



RC6(Render Standby)：

(Standby)Enable/disable integrated graphics standby, default Enabled.

MC6(Media Standby)：

(Standby)Enable/disable Media standby, default Enabled.

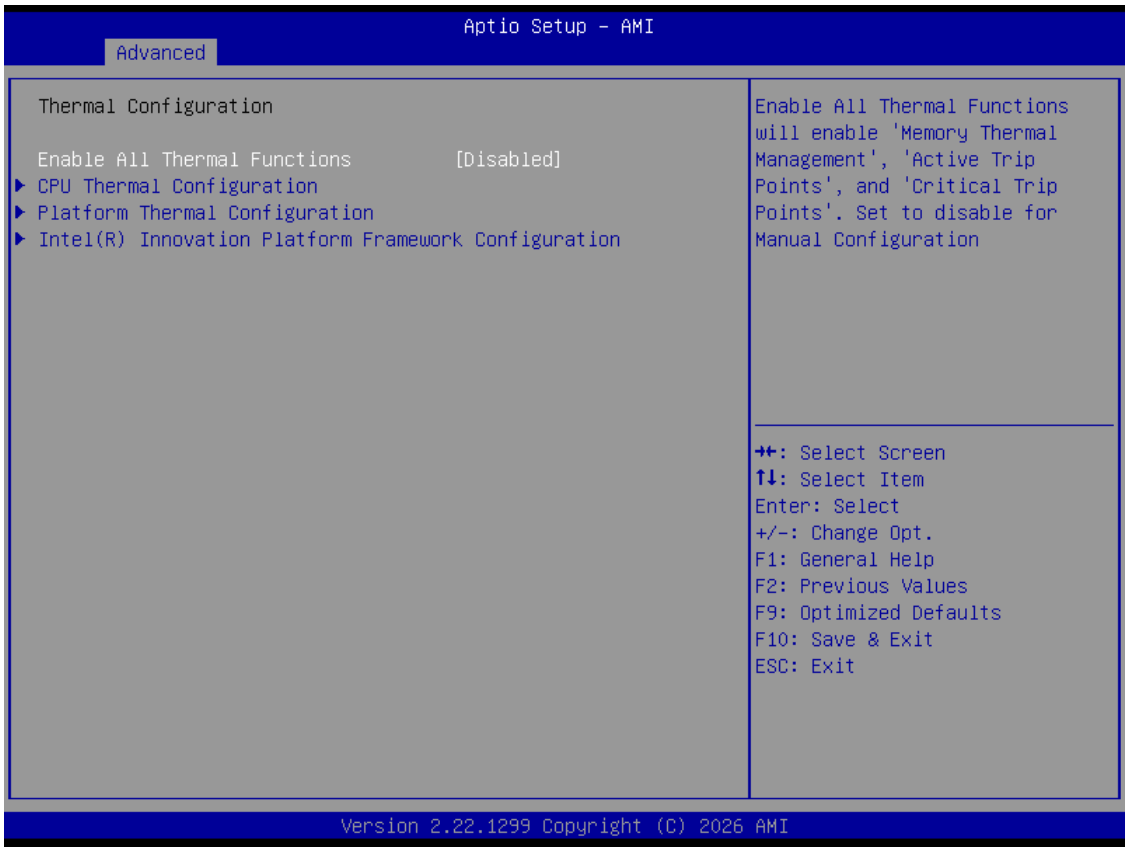
Maximum GT frequency：

Maximum GT Frequency, Default max frequency.

Disable Turbo GT frequency：

Disable Turbo GT Frequency mode, Default “Disabled”.

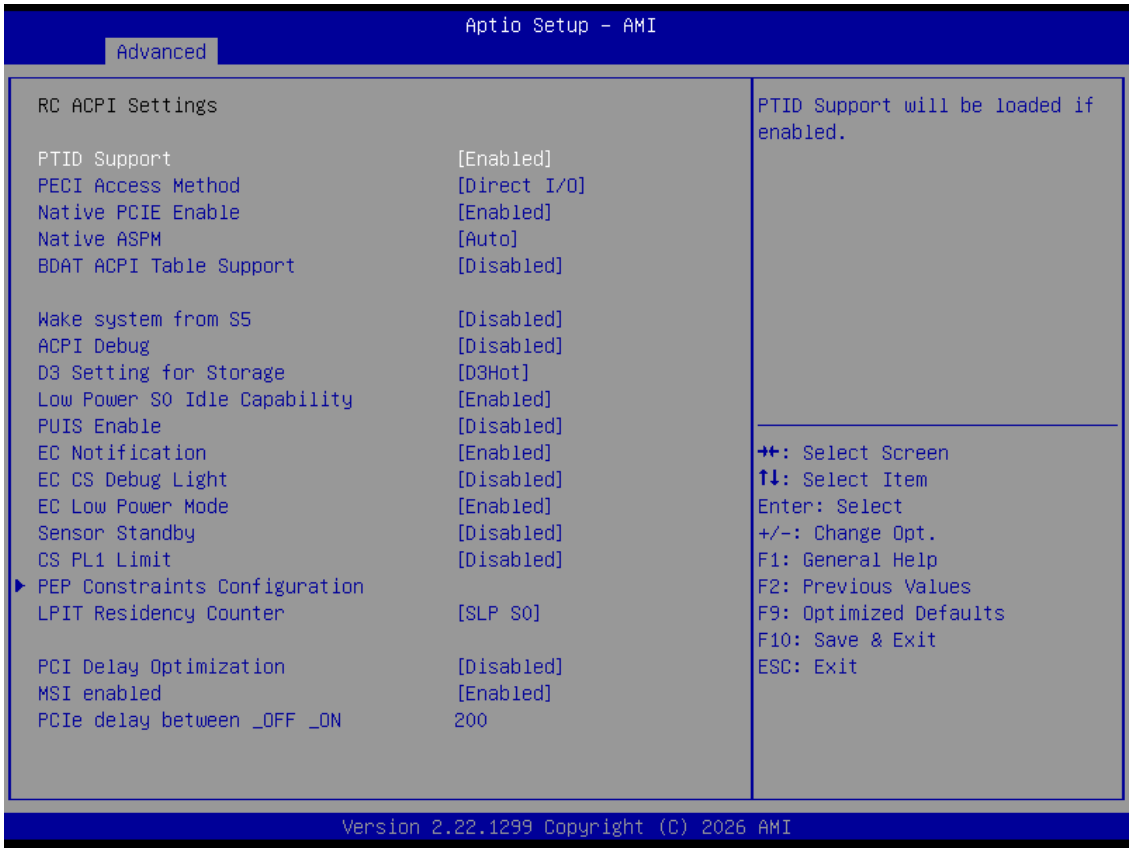
3.3.4 Thermal Configuration



The **Thermal Configuration** menu provides options for configuring the system's thermal management settings.

- **Enable All Thermal Functions** – Enables or disables all thermal management functions.
- **CPU Thermal Configuration** – Configures processor thermal management settings.
- **Platform Thermal Configuration** – Configures platform thermal management settings.
- **Intel(R) Innovation Platform Framework Configuration**– Configures Intel(R) Innovation Platform Framework.

3.3.5 RC ACPI Settings

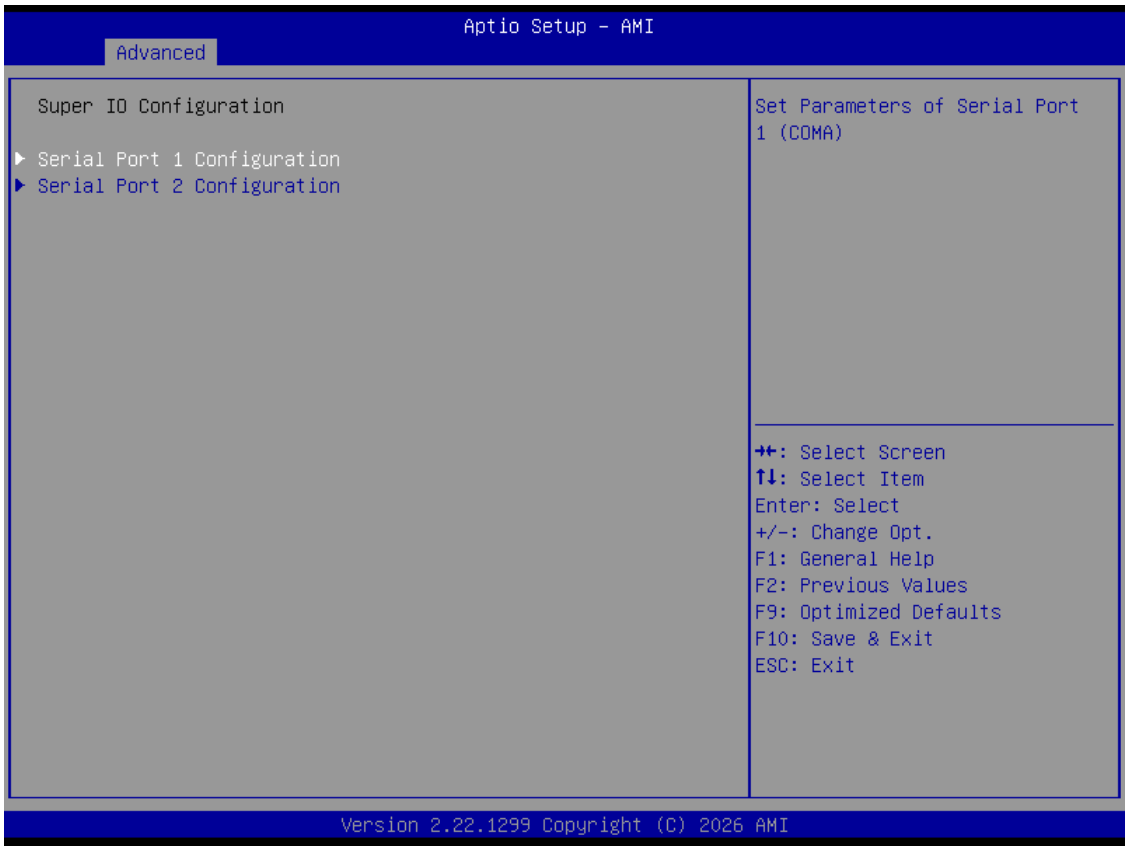


This menu allows you to configure ACPI power management and related platform settings.

- **PTID Support**: Enables or disables PTID support.
- **PECI Access Method**: Selects the access method for the Platform Environment Control Interface (PECI).
- **Native PCIE Enable**: Enables or disables native PCI Express support.
- **Native ASPM**: Configures PCI Express Active State Power Management (ASPM).
- **BDAT ACPI Table Support**: Enables or disables BDAT ACPI table support.
- **Wake system from S5**: Enables or disables system wake-up from the S5 (Soft Off) state.
- **ACPI Debug**: Enables or disables ACPI debugging.
- **D3 Setting for Storage**: Configures the D3 power state setting for storage devices.
- **Low Power S0 Idle Capability**: Enables or disables Low Power S0 Idle capability.
- **PUIS Enable**: Enables or disables Power-Up In Standby (PUIS).
- **EC Notification**: Enables or disables Embedded Controller (EC) notification.
- **EC CS Debug Light**: Enables or disables the EC CS debug light function.
- **EC Low Power Mode**: Enables or disables EC Low Power Mode.
- **Sensor Standby**: Enables or disables Sensor Standby.
- **CS PL1 Limit**: Enables or disables the CS PL1 Limit function.
- **PEP Constraints Configuration**: Configures Platform Extension Plug-in (PEP) constraints.

- **LPIT Residency Counter**: Selects the residency counter for the Low Power Idle Table (LPIT).
- **PCI Delay Optimization**: Enables or disables PCI delay optimization.
- **MSI enabled**: Enables or disables Message Signaled Interrupts (MSI).
- **PCIe delay between _OFF _ON**: Sets the delay between PCIe power-off and power-on operations.

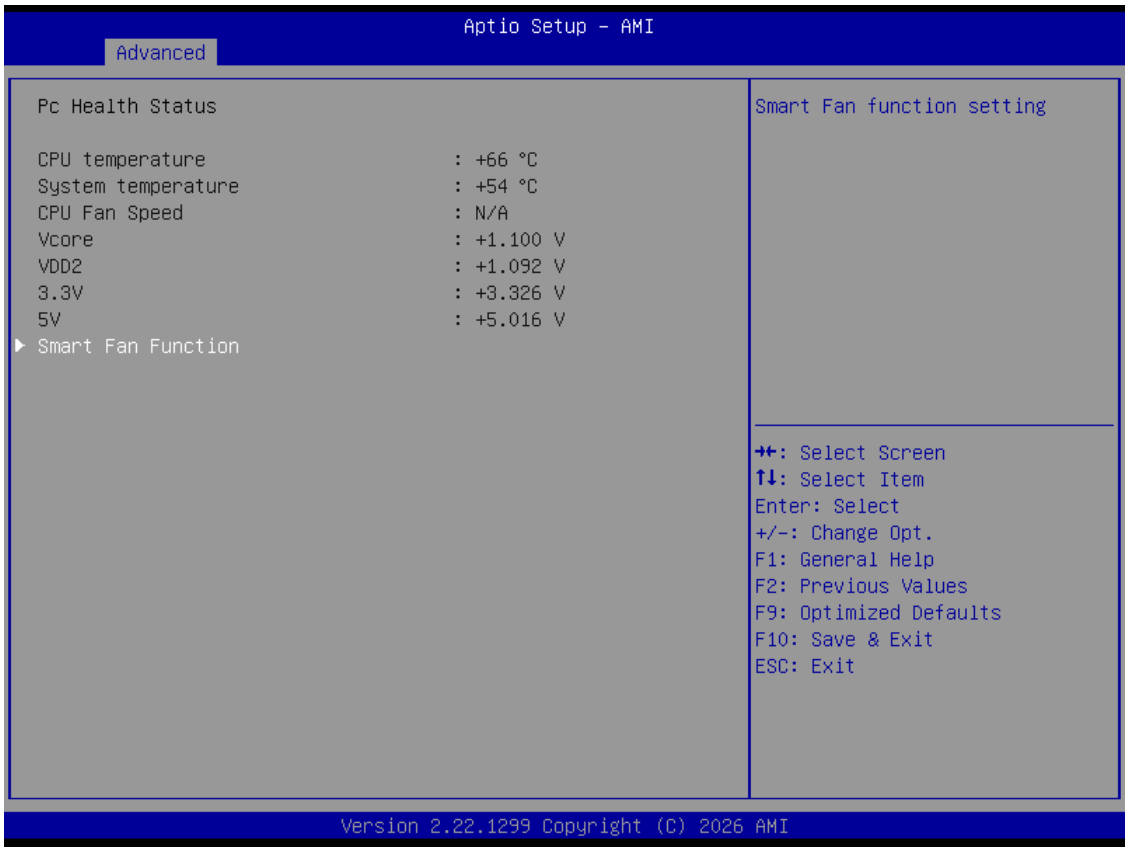
3.3.6 Super IO Configuration



The Super IO Configuration menu provides options for configuring the onboard serial ports.

- **Serial Port 1 Configuration:** Configures settings for serial ports COM1.
- **Serial Port 2 Configuration:** Configures settings for serial ports COM2.
- **Serial Port**:Enables or disables the selected serial port. Default: Enabled.
- **Device Settings:** Displays the I/O address and IRQ assigned to the selected serial port.
- **Change Settings:** Selects the I/O address and operating mode for the selected serial port.

3.3.7 Hardware Monitor

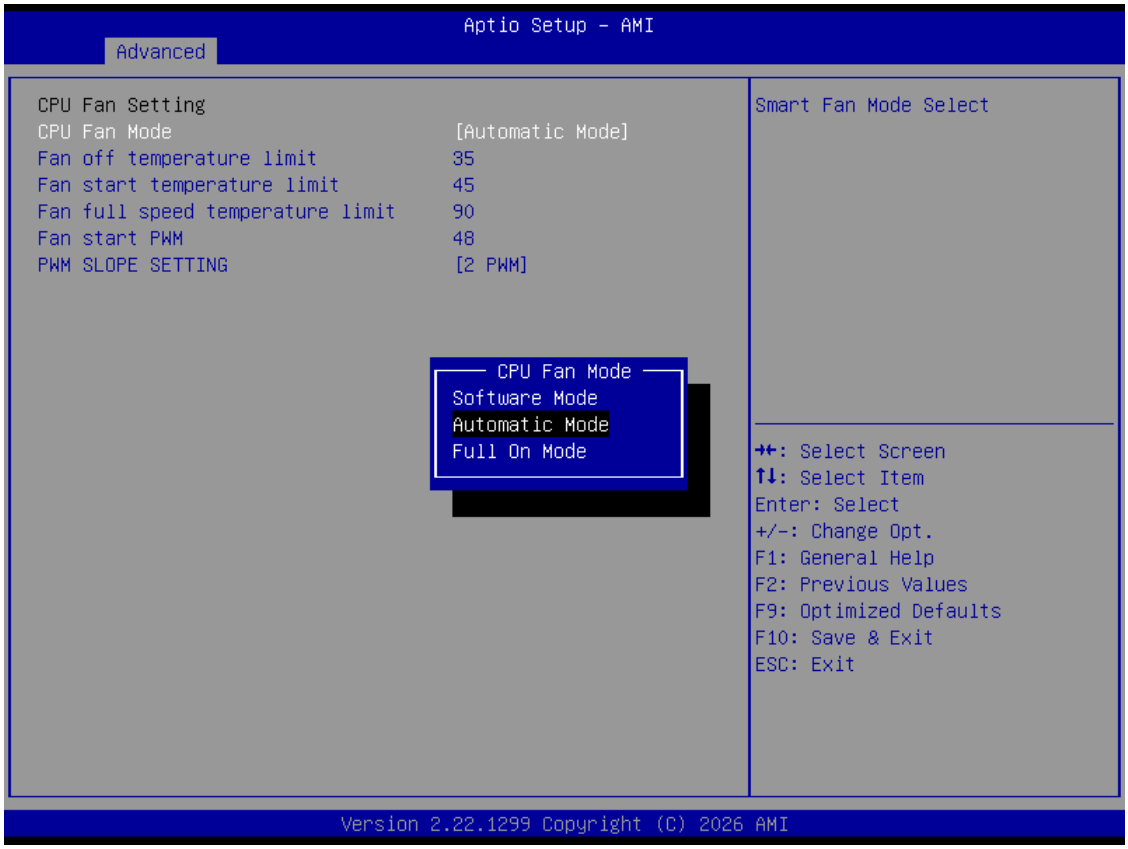


Advanced → Hardware Monitor → PC Health Status

The **PC Health Status** menu displays the current system health information, including temperatures, fan speed, and system voltages.

- **CPU Temperature**: Displays the current processor temperature.
- **System Temperature**: Displays the current system temperature.
- **CPU Fan Speed**: Displays the current CPU fan speed (RPM).
- **Vcore**: Displays the current processor core voltage.
- **VDDQ**: Displays the current memory I/O voltage (VDDQ).
- **3.3V**: Displays the current 3.3 V system voltage.
- **5V**: Displays the current 5 V system voltage.
- **Smart Fan Function**: Configures the system's smart fan control settings.

Smart Fan Function

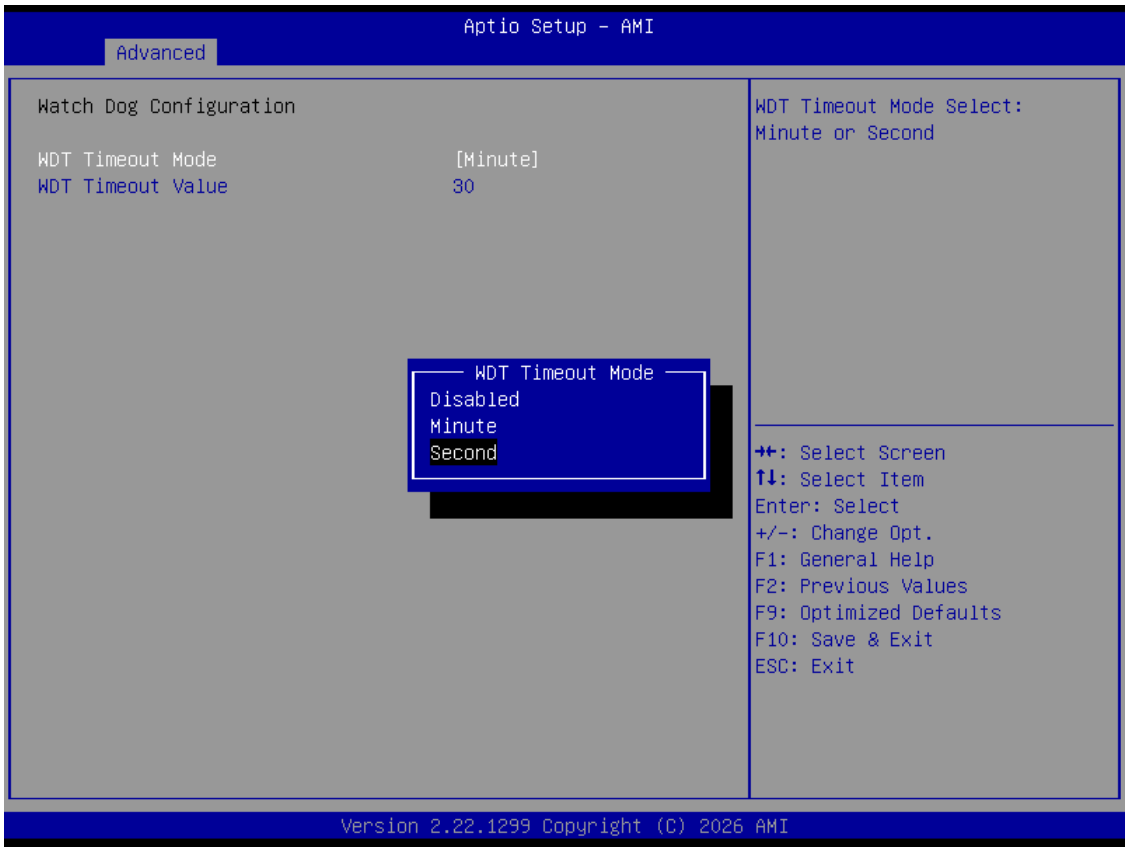


Advanced →Hardware Monitor →PC Health Status → Smart Fan Function → CPU Fan Setting

The **CPU Fan Setting** menu provides options for configuring the CPU fan control.

- **CPU Fan Mode**
  Selects the CPU fan control mode.
  - **Software Mode** – Allows manual configuration of the fan control parameters.
  - **Automatic Mode** – Automatically adjusts the fan speed according to the CPU temperature.
  - **Full On Mode** – Runs the CPU fan at maximum speed continuously.
- **Fan Off Temperature Limit**
  Sets the temperature below which the fan stops operating.
- **Fan Start Temperature Limit**
  Sets the temperature at which the fan starts operating.
- **Fan Full Speed Temperature Limit**
  Sets the temperature at which the fan reaches maximum speed.
- **Fan Start PWM**
  Sets the initial PWM duty cycle when the fan starts.
- **PWM Slope Setting**
  Adjusts the rate at which the PWM duty cycle increases as the temperature rises.

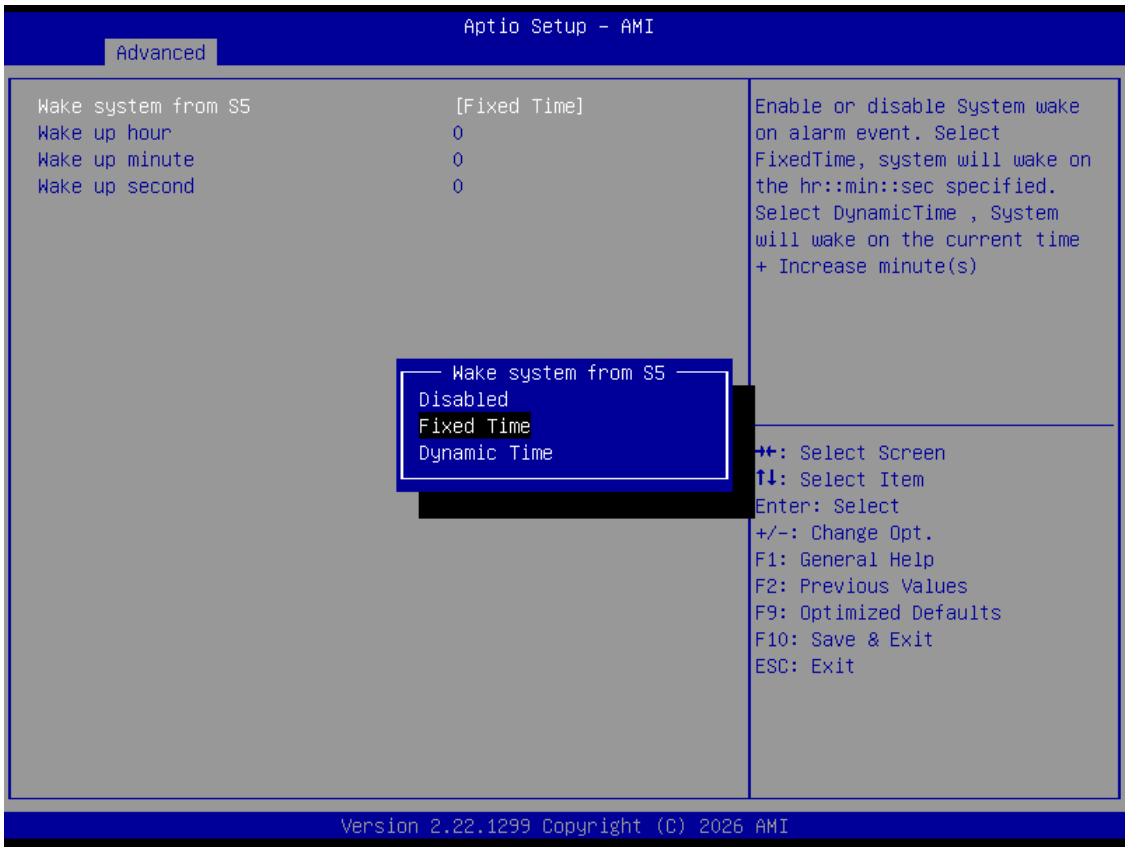
3.3.8 Watch Dog Configuration



Watch Dog Configuration

- WDT Timeout Mode select: Disabled/Minute/Second

3.3.9 S5 RTC Wake Settings



The S5 RTC Wake Settings menu allows the system to automatically power on from the S5 (Soft-Off) state using either a fixed schedule or a delayed timer.

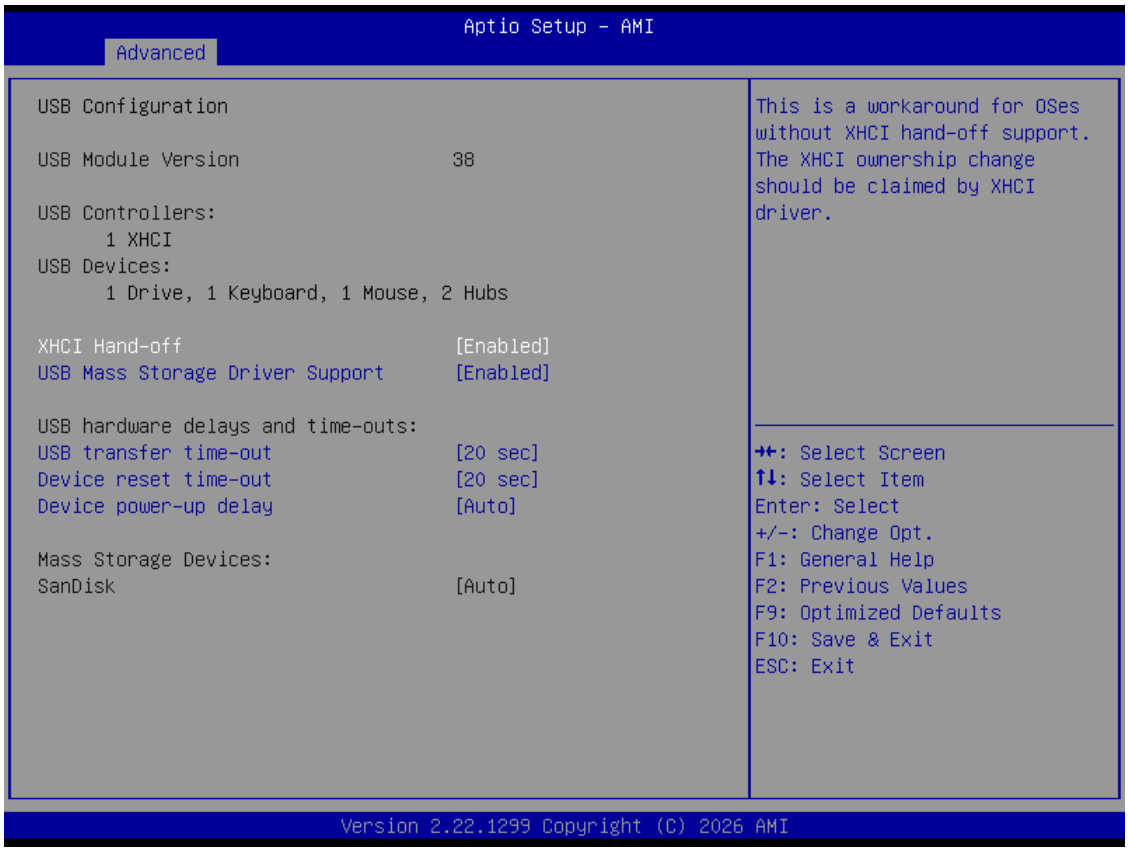
Wake System from S5: Enables or disables automatic system power-on from the S5 (Soft-Off) state.
Fixed Time: Schedules the system to power on at the same time every day while AC power is connected.

- Wake Up Hour – Sets the hour.
- Wake Up Minute – Sets the minute.
- Wake Up Second – Sets the second.

Dynamic Time: Schedules the system to power on after a specified delay from the current time.

Note: The automatic power-on function is available only while the system remains connected to AC power.

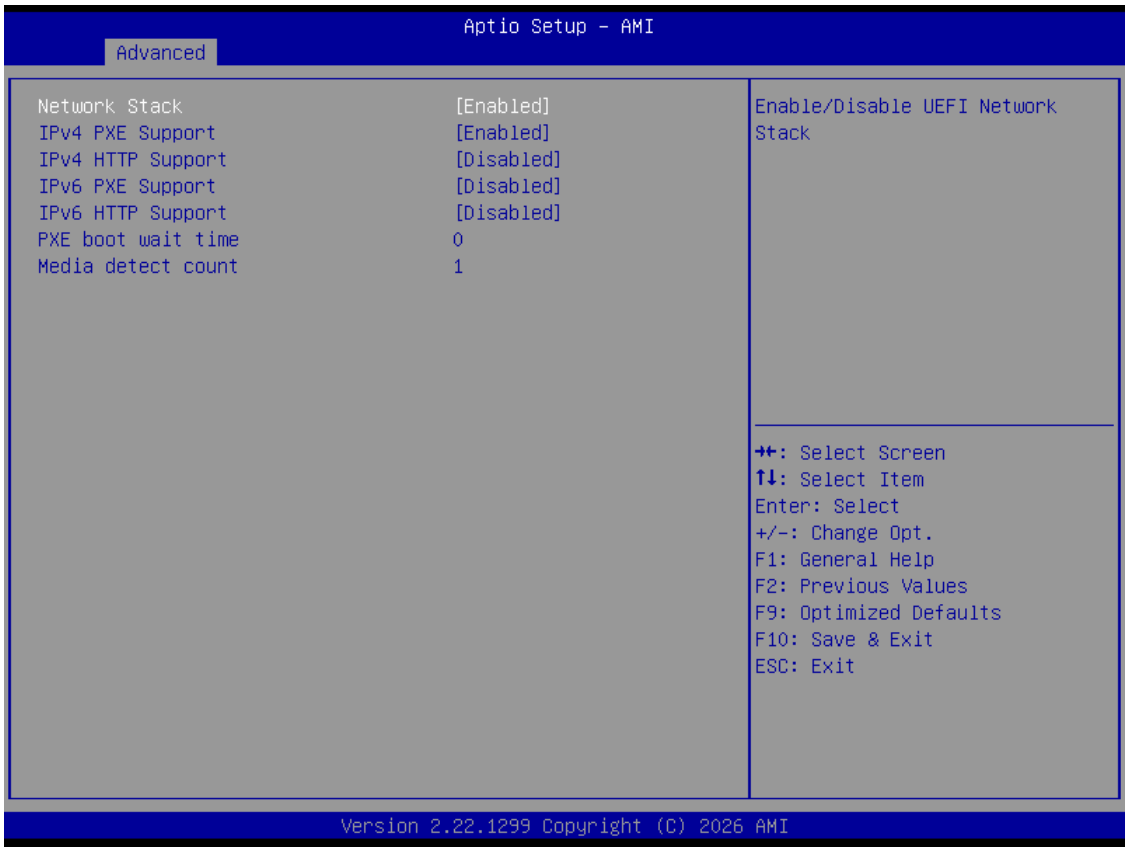
3.3.10 USB Configuration



The **USB Configuration** menu provides options for configuring USB controller settings and USB device support.

- **Legacy USB Support**: Enables or disables legacy USB support in the UEFI environment. When enabled, USB devices such as keyboards, mice, and USB storage devices can be used before the operating system loads.
- **XHCI Hand-off**: Enables or disables the xHCI hand-off function for operating systems that do not provide native xHCI driver support.
- **USB Mass Storage Driver Support**: Enables or disables support for USB mass storage devices. **Recommended:** *Enabled*.
- **USB3 Power Delivery during S5**: Enables or disables standby power to the USB 3.0 ports while the system is in the **S5 (Soft-Off)** state.
- **USB Transfer Time-out**: Sets the timeout value for USB control, bulk, and interrupt transfers. **Default:** *20 seconds*.
- **Device Reset Time-out**: Sets the timeout value for USB mass storage device reset operations during system startup. **Default:** *20 seconds*.
- **Device Power-up Delay**: Sets the maximum delay allowed for a USB device to become ready after power is applied.

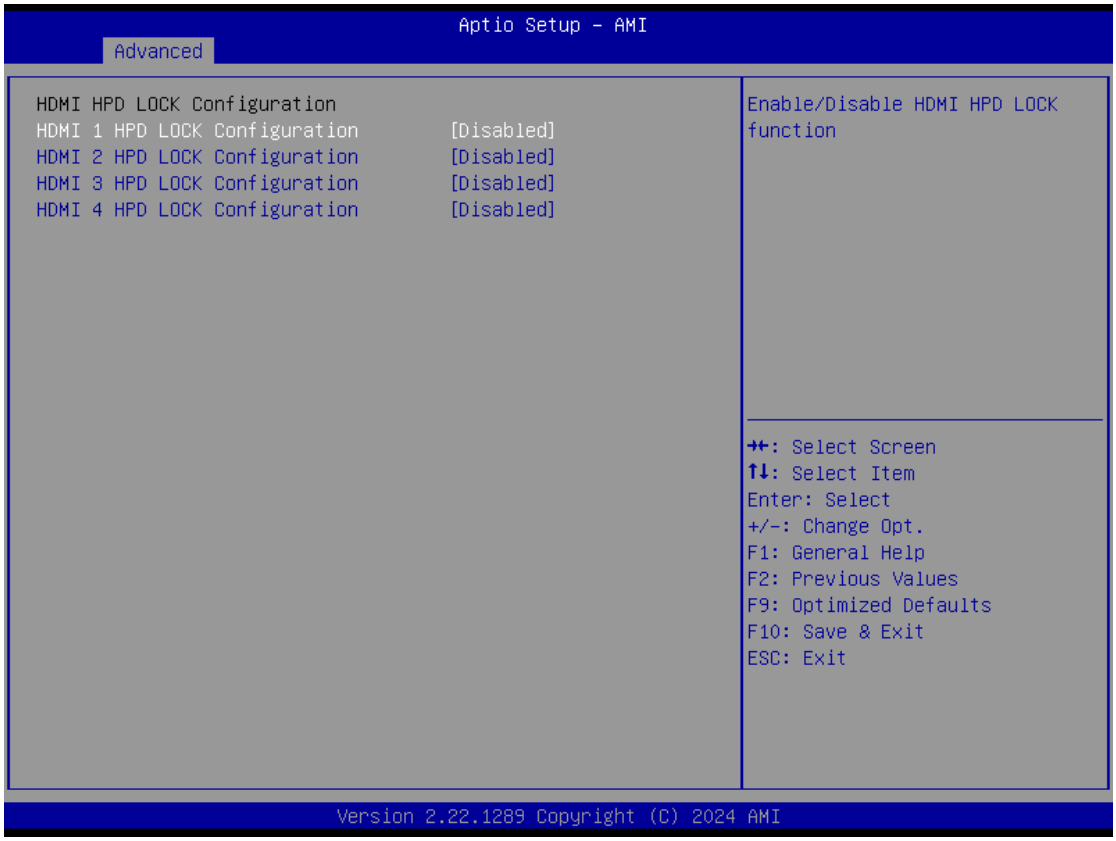
3.3.11 Network Stack Configuration



The **Network Stack Configuration** menu provides options for configuring the UEFI network stack and network boot features.

- **Network Stack**: Enables or disables the UEFI network stack for network boot.
  Default: *Disabled*.
- **IPv4 PXE Support**: Enables or disables PXE boot support over IPv4.
- **IPv4 HTTP Support**: Enables or disables HTTP boot support over IPv4.
- **IPv6 PXE Support**: Enables or disables PXE boot support over IPv6.
- **IPv6 HTTP Support**: Enables or disables HTTP boot support over IPv6.
- **PXE Boot Wait Time**: Sets the timeout before the PXE boot process starts.
- **Media Detect Count**: Sets the number of attempts to detect a network media connection before initiating network boot.

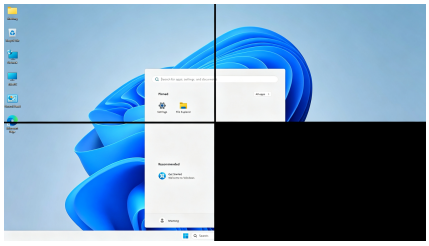
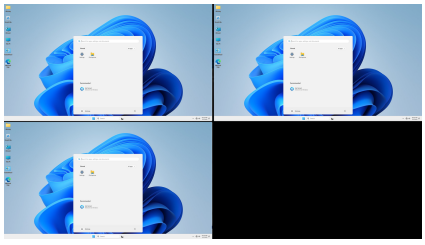
3.3.12 HDMI HPD LOCK Configuration



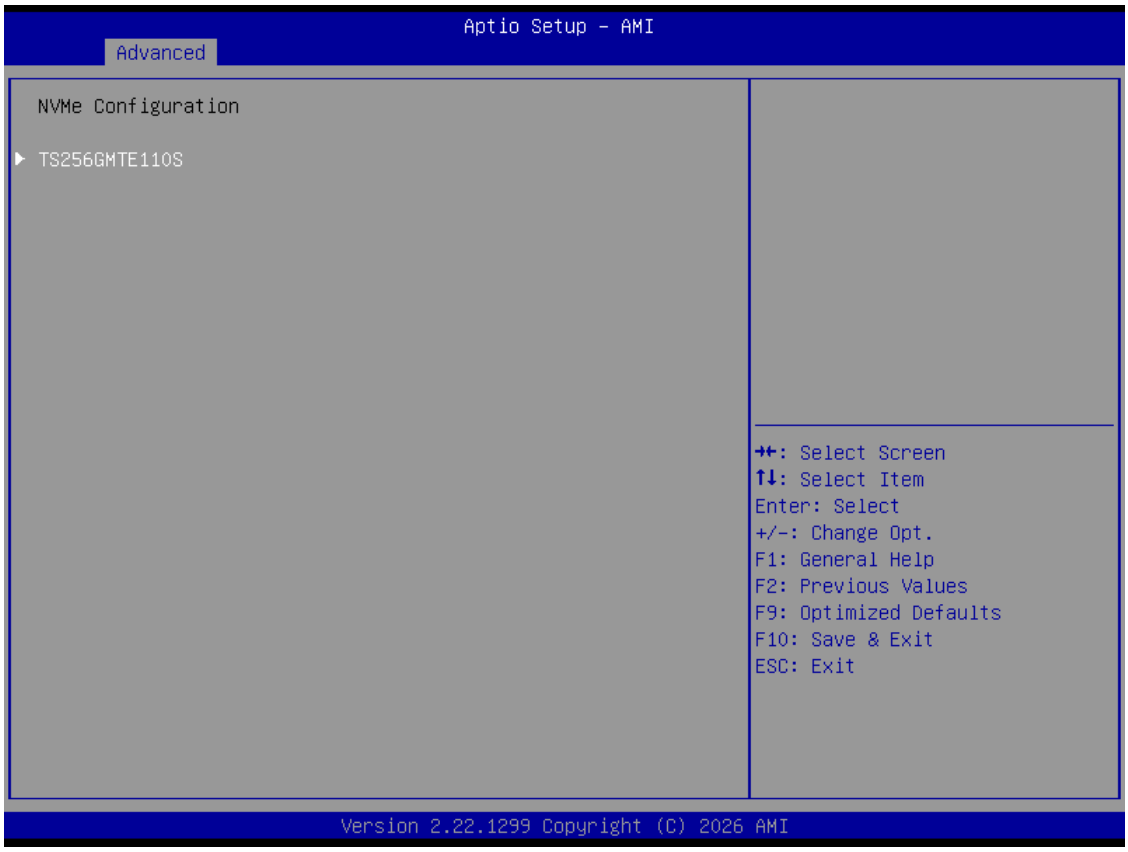
The **HDMI HPD LOCK Configuration** menu provides options for enabling or disabling the **HDMI Hot Plug Detect (HPD) Lock** function for each HDMI output.

- **HDMI 1 HPD LOCK Configuration**: Enables or disables the HPD Lock function for **HDMI 1**.
    - **Enabled** – Locks the HDMI display signal. **Disabled** – Disables the HDMI HPD Lock function.
- **HDMI 2 HPD LOCK Configuration**: Enables or disables the HPD Lock function for **HDMI 2**.
- **HDMI 3 HPD LOCK Configuration**: Enables or disables the HPD Lock function for **HDMI 3**.
- **HDMI 4 HPD LOCK Configuration**: Enables or disables the HPD Lock function for **HDMI 4**.

Note: *HDMI HPD Lock is intended for multi-display applications. When enabled, the system maintains the display configuration even if an HDMI cable is accidentally disconnected, helping prevent the desktop layout or display wall configuration from being interrupted.*

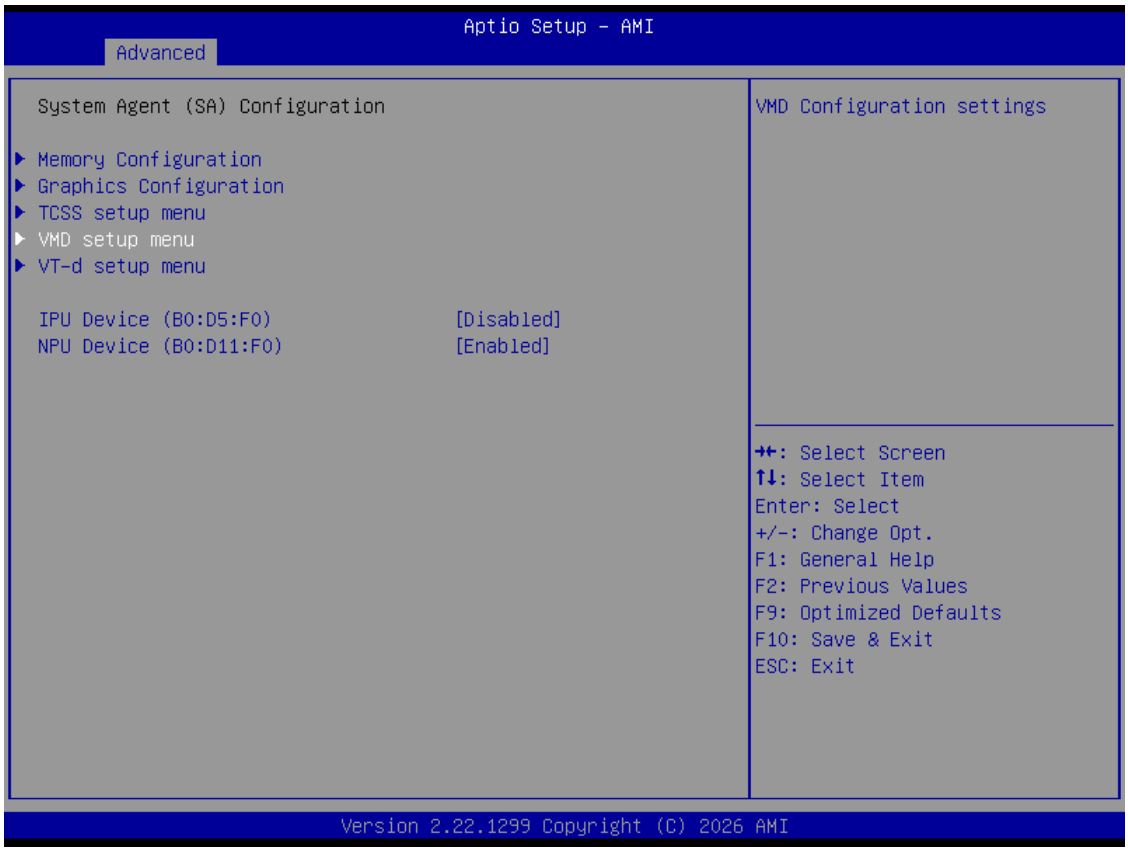
HDMI HPD LOCK Enabled	HDMI HPD LOCK Disabled
	

3.3.13 NVME Configuration



The **NVMe Configuration** menu displays information about installed **NVMe storage devices**. When a NVMe device is installed, the following information is displayed: Model Name, Storage Capacity

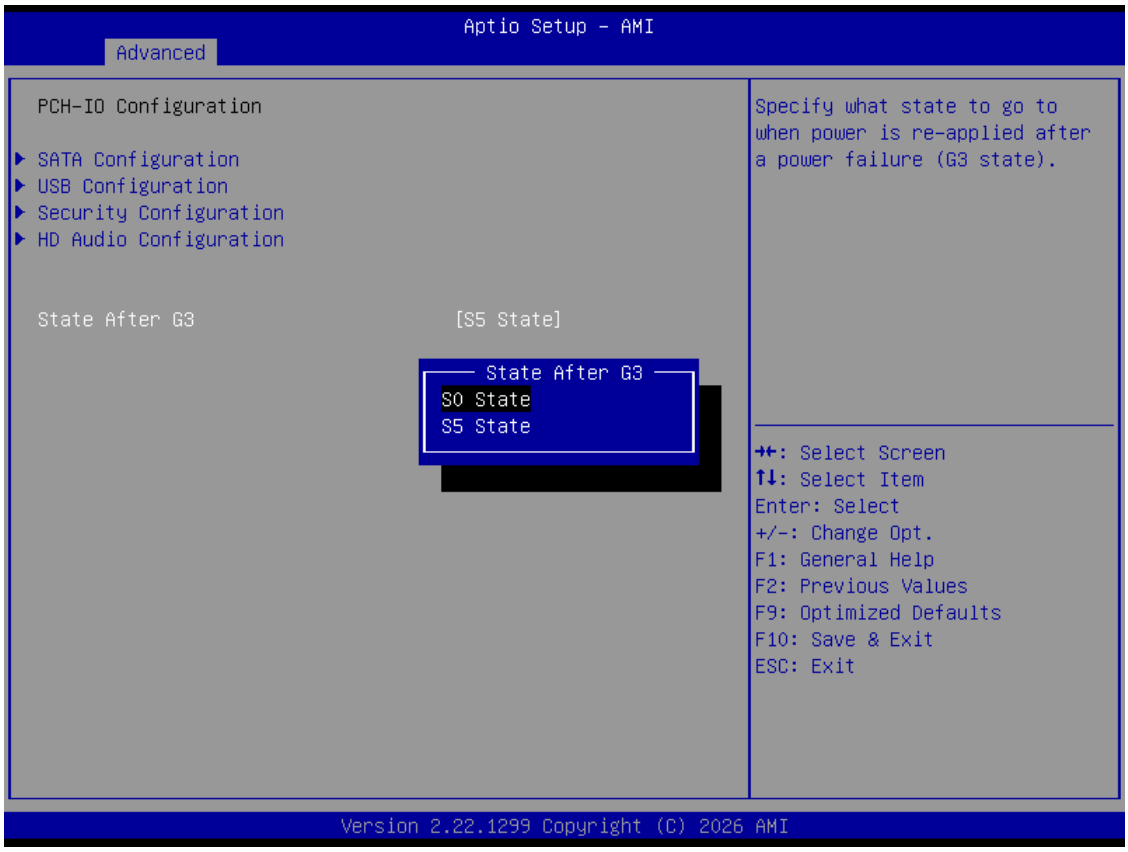
3.3.14 System Agent (SA) Configuration



The **System Agent (SA) Configuration** menu provides configuration options for memory, integrated graphics, TCSS, VMD, VT-d, and integrated processing devices.

- **Memory Configuration**: Displays memory information and provides memory-related configuration options.
- **Graphics Configuration**: Configures integrated graphics and display-related settings.
- **TCSS setup menu**: Configures Intel® Type-C Subsystem (TCSS) and related features.
- **VMD setup menu**: Configures Intel® Volume Management Device (VMD) and related storage settings.
- **VT-d setup menu**: Configures Intel® Virtualization Technology for Directed I/O (VT-d).
- **IPU Device**: Enables or disables the Intel® Image Processing Unit (IPU). Default: **Disabled**
- **NPU Device**: Enables or disables the Neural Processing Unit (NPU). Default: **Enabled**

3.3.15 PCH-IO Configuration



The **PCH-IO Configuration** menu provides configuration options for PCH I/O functions, including SATA, USB, security, audio, and system behavior after AC power is restored.

SATA Configuration: Configures SATA devices and related settings.

USB Configuration: Configures USB-related settings.

Security Configuration: Configures PCH-related security settings.

HD Audio Configuration: Configures the onboard HD Audio controller and related settings.

State After G3: Determines the system power state after AC power is restored following a power loss (G3 state).

- **S0 State** — The system automatically powers on when AC power is restored.
- **S5 State** — The system remains powered off when AC power is restored. **Default S5 State**

3.4 Security

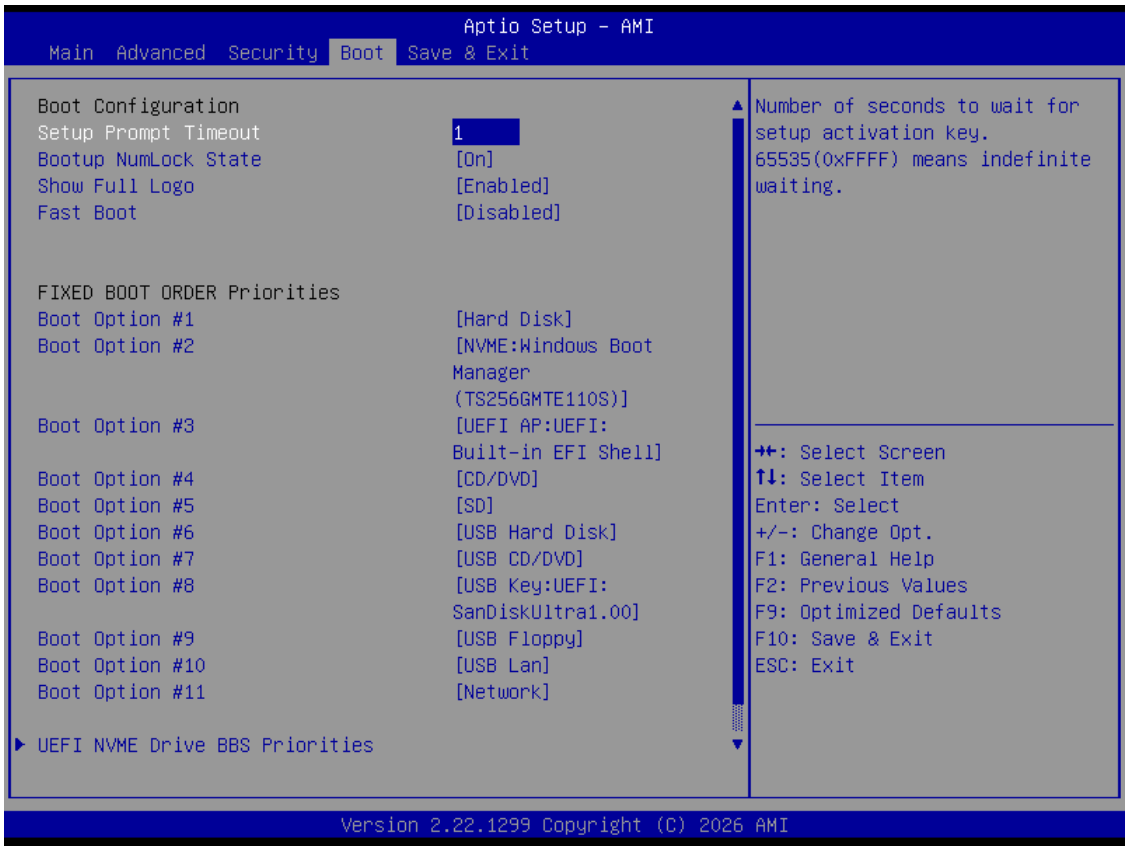


Administrator Password: Set the Administrator Password.

User Password: Set User Password.

Secure Boot: Configures Secure Boot settings.

3.5 BOOT



Boot Configuration

Setup Prompt Timeout: Sets the timeout period before the default boot option is initiated. A value of **0** starts the default boot option immediately, while **65535 (0xFFFF)** causes the firmware to wait indefinitely for user input before booting.

Bootup NumLock State: Selects the keyboard NumLock state after system startup.

- **On (Default):** Enables the numeric keypad for number entry.
- **Off:** Configures the numeric keypad to operate as cursor control keys.

Show Full Logo: Enables or disables the display of the customized boot logo.

- **Enabled:** Displays the boot logo.
- **Disabled:** Hides the boot logo.

Fast Boot: Enables or disables fast boot.

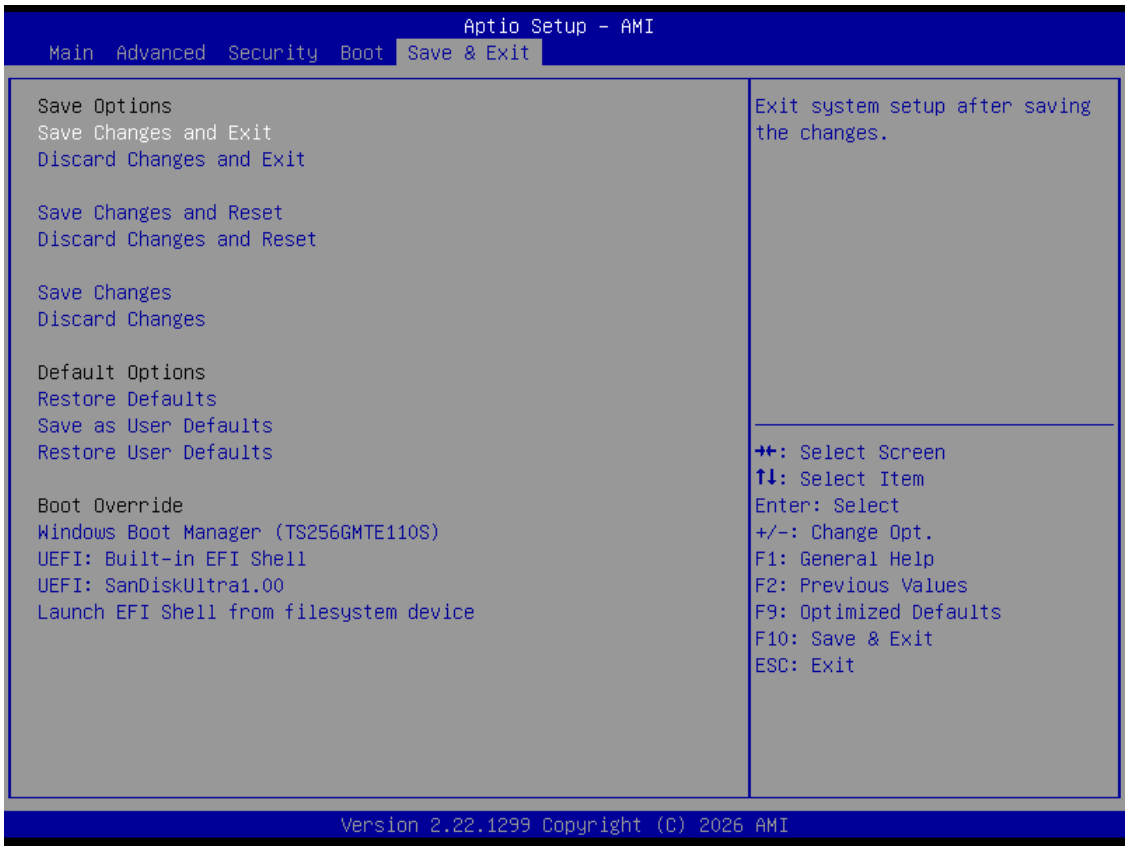
- **Enabled:** Enables fast boot
- **Disabled:** Disables fast boot

Boot Option #1–#11: Configures the boot priority order of available boot devices.

UEFI NVMe Drive BBS Priorities: Configures the boot priority of detected UEFI NVMe storage devices.

UEFI Application Boot Priorities: Configures the boot priority of UEFI applications.

3.6 Save & Exit



The **Save & Exit** menu provides options for saving or discarding BIOS configuration changes, restoring default settings, and selecting a temporary boot device.

- **Save Changes and Exit**: Saves all BIOS configuration changes and exits the BIOS Setup Utility.
- **Discard Changes and Exit**: Discards all unsaved BIOS configuration changes and exits the BIOS Setup Utility.
- **Save Changes and Reset**: Saves all BIOS configuration changes and restarts the system.
- **Discard Changes and Reset**: Discards all unsaved BIOS configuration changes and restarts the system.
- **Save Changes**: Saves the current BIOS configuration without exiting the BIOS Setup Utility.
- **Discard Changes**: Discards all unsaved BIOS configuration changes without exiting the BIOS Setup Utility.
- **Restore Defaults**: Restores the BIOS settings to the factory default values.
- **Save as User Defaults**: Saves the current BIOS configuration as the user-defined default settings.
- **Restore User Defaults**: Restores the previously saved user-defined default settings.

Boot Override

Boots the selected device immediately without changing the permanent boot order. Available devices may include SATA drives, USB storage devices, EFI Shell, PXE network boot, and other bootable devices

Appendix

GPIO Setting

Accessing GPIO70:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x01); //Bit0=1 set as output，bit0=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x01); // When set as output, Bit0 of I/O address 0xA06 = 1 outputs high level, Bit0 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit0=1 Set as output，bit0=0 Set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); //When set as input, Bit0 of I/O address 0xA06 reflects the read state.

Accessing GPIO71:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x02); // Bit1=1 set as output， bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x02); // When set as output, Bit1 of I/O address 0xA06 = 1 outputs high level, Bit1 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); // Bit0=1 set as output， bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit1 of I/O address 0xA06 reflects the read state.

Accessing GPIO72:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x04); //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x04); // When set as output, Bit2 of I/O address 0xA06 = 1 outputs high level, Bit2 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit2 of I/O address 0xA06 reflects the read state.

Accessing GPIO73:

Example: Accessing via IO

Set as output：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x08); //Bit3=1 set as output，bit3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x08); // When set as output, Bit3 of I/O address 0xA06 = 1 outputs high level, Bit3 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit3=1 set as output，bi3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit3 of I/O address 0xA06 reflects the read state.

Accessing GPIO74:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x10); //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x10); // When set as output, Bit4 of I/O address 0xA06 = 1 outputs high level, Bit4 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit4 of I/O address 0xA06 reflects the read state.

Accessing GPIO75:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x20); //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x20); // When set as output, Bit5 of I/O address 0xA06 = 1 outputs high level, Bit5 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit5 of I/O address 0xA06 reflects the read state.

Accessing GPIO76:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x40); //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x40); // When set as output, Bit6 of I/O address 0xA06 = 1 outputs high level, Bit6 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e (0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit6 of I/O address 0xA06 reflects the read state.

Accessing GPIO77:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x80); //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x80); // When set as output, Bit7 of I/O address 0xA06 = 1 outputs high level, Bit7 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit7 of I/O address 0xA06 reflects the read state.