User Manual

FP-710 V1.0



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FP-710
User Manual

(Version1.0)

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Warning

1. Before using the product, carefully read the manual to ensure proper installation and operation.
2. If you are not ready to install any extension card, store it in an anti-static protective bag to prevent damage.
3. To discharge any static electricity, briefly touch a grounded metal object before removing the extension card from the protective bag.
4. Always wear anti-static gloves and handle the card by its edges to avoid damaging sensitive components.
5. Verify that the power supply voltage is correct before connecting the motherboard to the power supply.
6. To prevent electric shock or damage, always turn off the AC power or unplug the power cord before removing or reconfiguring the motherboard or any components.
7. Unplug the AC power cord from the outlet before relocating the motherboard or any components.
8. Ensure all power cords are unplugged before connecting or disconnecting any equipment to avoid electrical hazards.
9. Wait at least 30 seconds after powering off the system before powering it on again to prevent unnecessary wear.
10. If any issues arise during operation, consult a qualified professional for assistance.
11. This product may cause radio interference in certain environments; if necessary, users should take appropriate measures to mitigate such interference.

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Chapter 1 Product Introduction

1.1 Brief Introduction

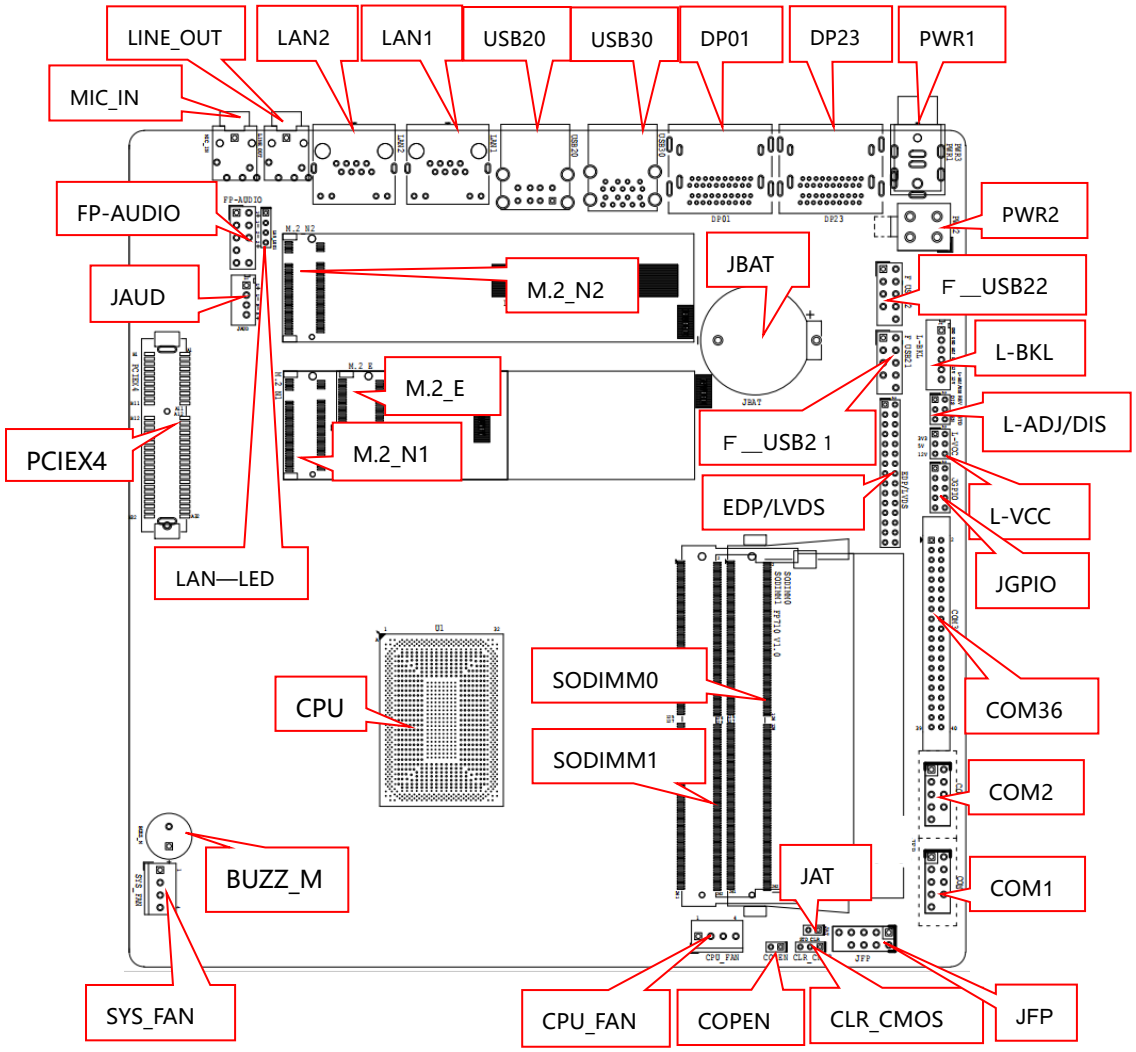
The FP-710 motherboard is a mini-ITX motherboard based on the AMD Ryzen PRO platform.

1.2 Parameters

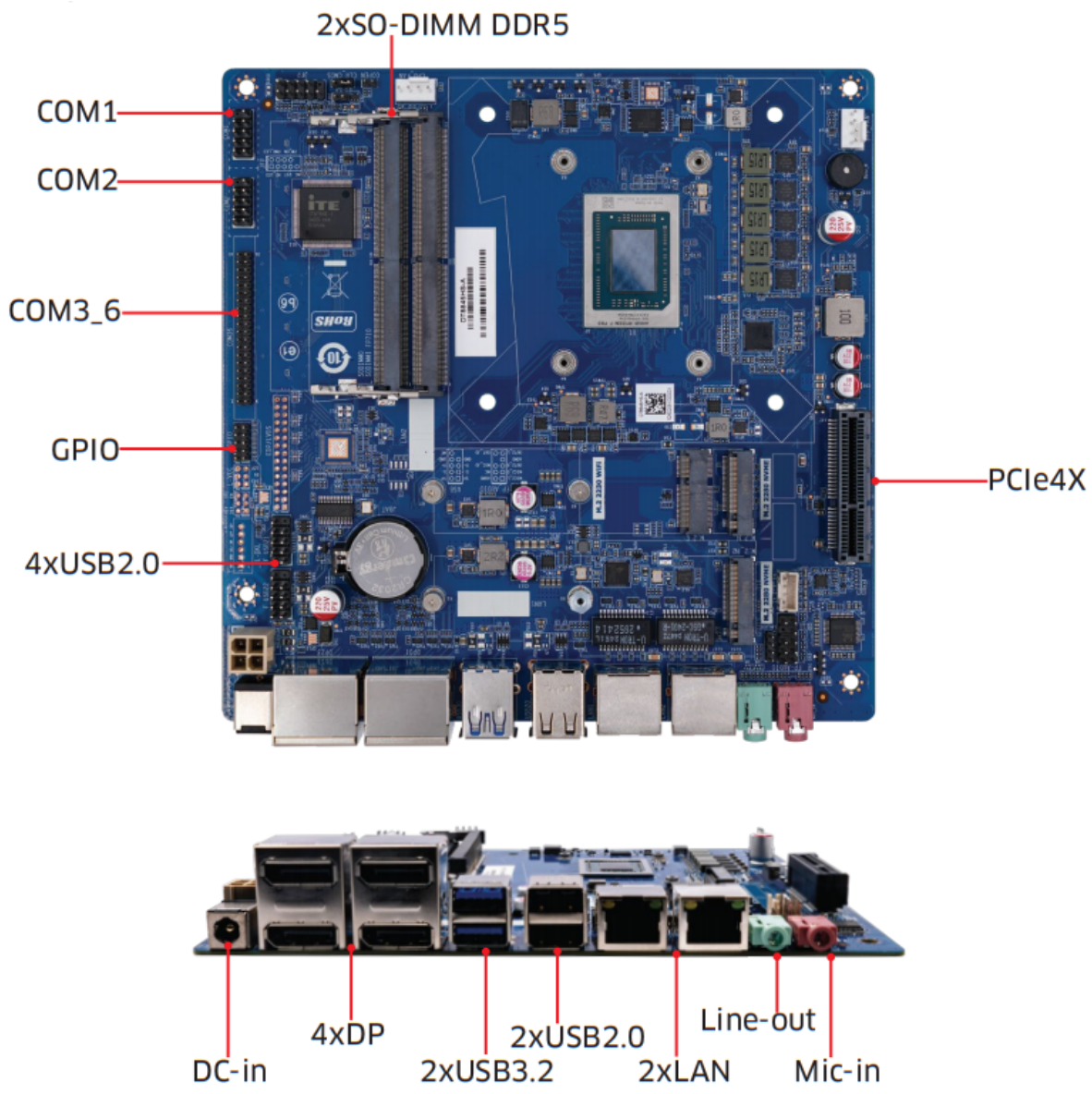
CPU	Ryzen™ 7 PRO 8845HS	8 Cores 16 Threads. Max. Boost Clock Up to 5.1 GHz. Base Clock 3.8 GHz. 8MB L2 Cache, 16MB L3 Cache. Default TDP 45W, cTDP 35-54W.
NPU	AMD Ryzen™ AI	Performance: Up to 16 TOPS, Overall TOPS: Up to 38 TOPS, NPU TOPS: Up to 16 TOPS.
RAM	2 x SO-DIMM DDR5-5600MHz, Support Dual Channels, up to 96GB	
GPU	AMD Radeon™ 780M	Graphics Core Count: 12, Graphics Frequency: 2700 MHz
Display Interface	4xDP1.4 Rear Ports 1xLVDS/EDP (optional, onboard pin)	
Storage	2xM.2 Key M Slots for 2280 NVMe SSD (labeled M.2_N1, M.2_N2 onboard)	
Audio	Realtek® ALC897 High-Definition Audio Codec. 1xLine-out, 1xMic-in.	
Ethernet	2x RJ45 LAN LAN1: Realtek® RTL8125BG. Max.Speed:10/100/1000/2500Mbps(2.5Gbps) LAN2: Realtek® RTL8111H. Max.Speed:10/100/1000Mbps(1.0Gbps)	
USB	2xUSB3.2 TYPE A GEN2 10 Gbps, 2xRear ports (labeled USB30 onboard) 6xUSB2.0 TYPE A 480Mbps, 2xRear ports (labeled USB20 onboard), 4xHeaders 2.54mm pitch (labeled F_USB21/F_USB22 onboard)	
Expansion	• 1 x M.2 Key E Slot for 2230 WiFi & BT modules (Labeled M.2_E onboards, support PCIe/USB 2.0) • 1 x PCI-E x4 (Labeled PCIeX4 onboard)	
COM	6x COM headers, RS232 by default. COM2 can be optionally configured as RS485 through hardware changes. Labeled COM1/COM2 (2.54 mm pitch) / COM36 (2.0 mm pitch) onboard.	
GPIO	8-bit GPIO header (labeled JGPIO onboard, 2.0 mm pitch)	
TPM	External TPM module (optional, supports Infineon SLB9670 TPM chip)	
Buzzer	Onboard buzzer (labeled BUZZ_M onboard)	
Other	• COPEN detection header (labeled COPEN onboard, 2.0 mm pitch)	

	• JFP front panel header (labeled JFP onboard, 2.54 mm pitch) • JAT auto power-on header (labeled JAT onboard, 2.0 mm pitch) • LAN activity LED header (labeled LAN_LED onboard, 2.0 mm pitch) • Front audio header (labeled F_AUDIO onboard, 2.54 mm pitch) • JAUD amplifier header (labeled JAUD onboard, 2.0 mm pitch) • 12V 4-pin CPU fan header (labeled CPU_FAN onboard) • 12V 4-pin system fan header (labeled SYS_FAN onboard) • Clear CMOS header (labeled CLR_CMOS onboard)
Power	12V DC-IN (5.25 mm jack); optional: 19V DC-IN (5.25 mm jack
Dimension	Mini ITX Form Factor, Size 170 mm x 170 mm
CPU Cooler Compatibility	Compatible with Intel® LGA115X Socket Coolers Only
Temperature	Operating Temp. -20°C ~60°C Storage Temp. -40°C ~80°C

1.3 Connector Diagram



1.4 I/O Interfaces



Chapter 2 Hardware

2.1 Installations

Please refer to the following steps for installation:

1. Read the user manual carefully to make sure all the adjustments on FP-710 are correct.
2. Installing the Memory:
    - Press the ejector tab of the memory slot outwards with your fingertips.
    - Hold the memory module and align the key to the module with that on the memory slot.
    - Gently push the module into the slot until the ejector levers return completely to the closed position, holding the module in place when the module touches the bottom of the slot. To remove the module, press the ejector levers outwards to unseat the module.
3. Installing the expansion cards:
    - Locate the expansion slots and remove the screw, insert the cards into the slot at a 45-degree angle then attach the screw to the expansion cards, gently press down on it then install the screw back.
4. Connect all signal wires, cables, panel control wiring, and power supplies.
5. Start the computer and complete the setup of the BIOS program.

Attention!!!

The Motherboard's components are integrated circuits and can easily be damaged by Electrostatic Discharge or ESD; therefore, please follow the instructions:

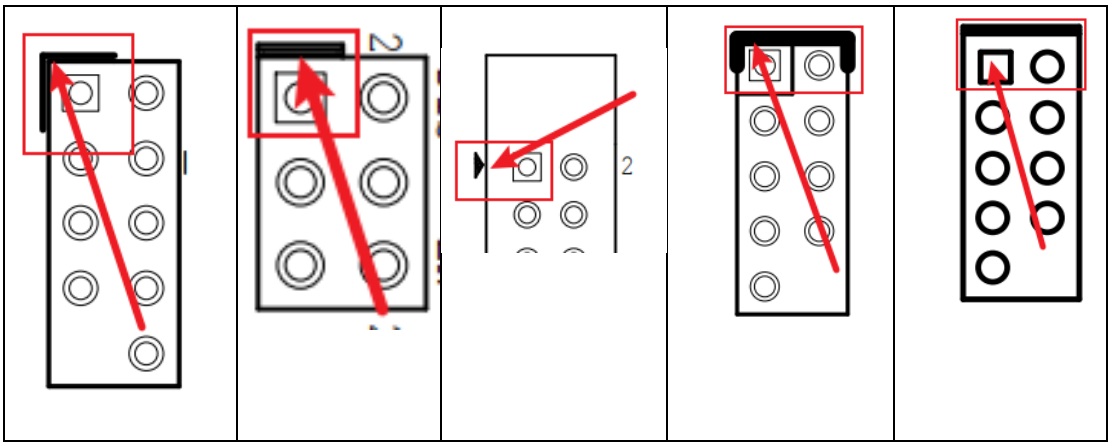
- Hold the board's edge when handing, and do not touch onboard pins, components, or plug sockets.
- When touching integrated circuit components (such as CPU, RAM, etc.), please wear an anti-static wrist strap/glove to avoid electrostatic discharge damage to the board or other sensitive components.
- Before installing the integrated circuits/sensitive components, place the sensitive components in anti-static bags to keep them safe from ESD.
- Please make sure the power switch is OFF before plugging the power plug.

2.2 Jumper Setting

Before installing hardware devices, configure the corresponding jumpers according to your needs using the table below.

Identifying Jumper/Pin "1": Observe the text markings next to jumpers or pins, which may indicate pin "1" with the number '1', bold lines, or triangle symbols (as shown below); alternatively, examine the solder pads on the reverse side—square pads denote pin "1".

Illustration:



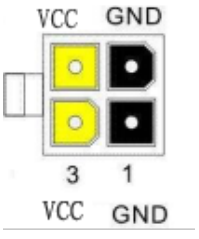
2.3 Memory Slots

The board provides two SO-DIMM DDR5-5600 MHz slots and supports dual-channel memory with a maximum capacity of up to 96 GB.

Note!! When installing memory modules, carefully hold the module by its edges and align the notch (key) on the module with the key in the slot. Ensure that the selected memory module matches the board's specifications to ensure optimal performance and compatibility.

2.4 Board Power Supply (labeled PWR1, PWR2 onboard)

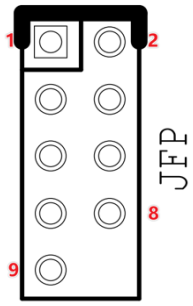
The board supports a 12V/19V(optional) DC-IN via 5.25 mm DC jack or ATX auxiliary power input (2x2 pin).

PWR1: DC adapter power jack	**PWR2:** ATX auxiliary power connector (2x2 pin)
	

2.5 Front Panel Header (labeled JFP onboard)

The front panel header connects to the function buttons and indicator LEDs located on the chassis front panel.

Pin Definition (JFP):



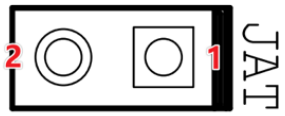
Signal	Pin		Signal
HDD_LED+	1	2	PWR_LED+
HDD_LED-	3	4	PWR_LED-
RSTBTN-	5	6	PWR_ON+
RSTBTN+	7	8	PWR_ON-
NUL	9	10	(null)

2.6 Auto Power-On (labeled JAT onboard)

The JAT header enables or disables the *auto power-on* function.

Configure the jumper as follows:

Enable Auto Power-On	Disable Auto Power-On
1-2	NC



2.7 CMOS Clearance/Retention (labeled CLR_CMOS onboard)

CMOS is powered by onboard button batteries. Clearing CMOS will permanently remove the previous system settings and restore the board system to original settings (factory settings).

Step 1: Turn off the PC and disconnect the power.

Step 2: Press CLR_CMOS for 15 seconds then disconnect.

Step 3: Restart the device, press the <DEL> button to enter the BIOS, load the optimal default value, save, and exit the settings.

CLR_CMOS (Insert the corresponding jumper cap to enable the corresponding function):

CLR _CMOS	NC
1-2	2-3



⚠**Attention!!!** Do not clear the CMOS while the PC/Board is powered on, as this may damage the motherboard.

2.8 Display Interfaces

The board features 4x DisplayPort 1.4 (DP) ports, each supporting up to 4K at 120 Hz.

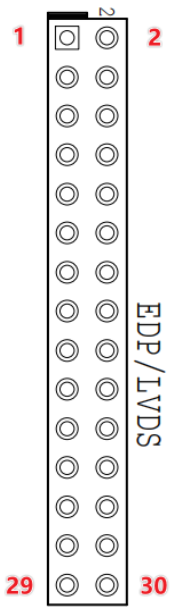
It also includes 1x LVDS/eDP header, supporting up to 1920×1200 at 24-bit (optional).

Note: When the LVDS/eDP header is in use, the DP0 channel will be occupied, and the DP0 port will be disabled.

2.8.1 LVDS (labeled EDP/LVDS, L-BKL, L-ADJ/DIS, L_VCC onboard)

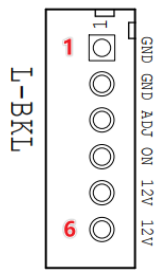
When set to LVDS mode, the “EDP/LVDS” pins output LVDS signals. The “L-BKL” pins are used for backlight control, and the “L_VCC/BKL” pins provide power to the panel and backlight (with forward/inversion adjustment).

LVDS Data Pins (labeled EDP/LVDS onboard):



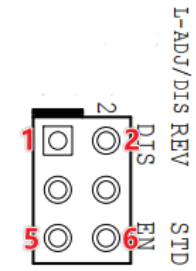
Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	GND
GND	5	6	GND
A_DATA0_DN	7	8	A_DATA0_DP
A_DATA1_DN	9	10	A_DATA1_DP
A_DATA2_DN	11	12	A_DATA2_DP
GND	13	14	GND
A_CLK_DN	15	16	A_CLK_DP
A_DATA3_DN	17	18	A_DATA3_DP
B_DATA0_DN	19	20	B_DATA0_DP
B_DATA1_DN	21	22	B_DATA1_DP
B_DATA2_DN	23	24	B_DATA2_DP
GND	25	26	GND
B_CLK_DN	27	28	B_CLK_DP
B_DATA3_DN	29	30	B_DATA3_DP

LVDS Backlight Connector Pin (Labeled L-BKL onboard):



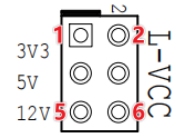
Pin	Singal
1	GND
2	GND
3	LCD_BKL_ADJ
4	LCD_BKL_ON
5	12V
6	12V

LVDS Backlight Adjustment Pin (Forward/Reverse) / LVDS Switch Pin (Labeled L-ADJ/DIS onboard)



Pin	Setting	Function
2-4	Close	REV (Backlight Control Reverse)
4-6	Close	STD (Backlight Control Standard)
1-3	Close	DIS (Disable LVDS)
3-5	Close	EN (Enable LVDS)

LVDS Operating Voltage Adjustment Pin (labeled L_VCC onboard)



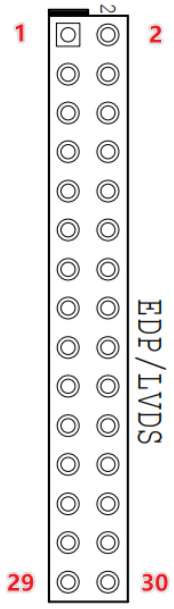
Pin	Setting	Function
1-2	Close	VCC 3.3V
3-4	Close	VCC 5V
5-6	Close	VCC 12V (Same output voltage as DC power supply)

Note: The LVDS operating voltage adjustment switch is pin-controlled. By shorting the jumper caps, the voltage can be flexibly adjusted between 3.3V/5V/12V. Based on your LVDS display's voltage parameters, use the jumper caps to short the pins corresponding to the required voltage. (Do not short pins of different voltages simultaneously.)

2.8.2 eDP(optional)

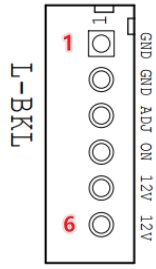
When set to eDP mode, the “EDP/LVDS” pins output eDP signals. The “L-BKL” pins are used for backlight control, and the “L-ADJ/DIS” pins provide power to the panel and backlight (with forward/inversion adjustment).

eDP Data Pins(labeled EDP/LVDS onboard):



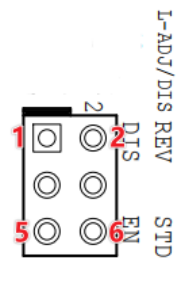
Singal	Pin		Singal
VCC	1	2	VCC
VCC	3	4	EDP_HPD
GND	5	6	GND
EDP_AUXN	7	8	EDP_AUXP
N/A	9	10	N/A
EDP_DATA0_P	11	12	EDP_DATA0_N
GND	13	14	GND
N/A	15	16	N/A
EDP_DATA1_P	17	18	EDP_DATA1_N
N/A	19	20	N/A
N/A	21	22	N/A
N/A	23	24	N/A
GND	25	26	GND
N/A	27	28	N/A
N/A	29	30	N/A

eDP Backlight Connector Pin (labeled L-BKL onboard):



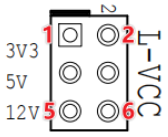
Pin	Singal
1	GND
2	GND
3	LCD_BKL_A
4	LCD_BKL_O
5	12V
6	12V

eDP Backlight Adjustment Pin (Forward/Reverse)/eDP Switch Pin (Labeled L-ADJ/DIS onboard)



Pin	Setting	Function
2-4	Close	REV((Backlight Control Reverse)
4-6	Close	STD (Backlight Control Standard)
1-3	Close	DIS (Disable eDP)
3-5	Close	EN (Enable eDP)

eDP Operating Voltage Adjustment Pin (labeled L_VCC onboard):



Pin	Setting	Function
1-2	Close	VCC 3.3V
3-4	Close	VCC 5V
5-6	Close	VCC 12V (Same output voltage as DC power supply)

Note: The eDP operating voltage adjustment switch is pin-controlled. Jumper caps can be used to flexibly adjust between 3.3V/5V/12V. Based on your eDP display's voltage specifications, use jumper caps to short the pins corresponding to the required voltage.(Do not short pins of different voltages simultaneously.)

2.9 Storage Interfaces (labeled M.2_N1/ M.2_N2 onboard)

The board features 2xM.2_key M slots (labeled M.2_N1/M.2_N2 onboard) for 2280 NVMe SSDs.

2.10 USB Interfaces (labeled USB30, USB20, F_USB21, F_USB22 onboard)

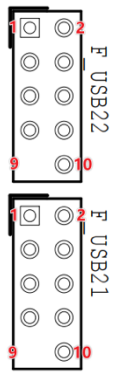
The board features

- 2x USB 3.2 Gen 2 Type-A ports (10 Gbps, labeled USB30 onboard)
- 2x USB 2.0 Type-A ports (480 Mbps, labeled USB20 onboard)

The rear USB 2.0 Type A port (labeled “USB20” onboard) is powered by a 5V standby voltage. It can wake the system from shutdown (non-power-off) or sleep states via a USB keyboard/mouse connected to the corresponding port and can also supply power to external devices: 5V/0.5A.

- 2x USB 2.0 headers (labeled F_USB21/F_USB22 onboard). Each header supports 2 ports, up to 4 × USB 2.0 Type-A (480 Mbps).

USB Pin definition(labels F_USB21/F_USB22 onboard):



Singal	**Pin**		**Singal**
VCC 5V	1	2	VCC 5V
USB DATA-	3	4	USB DATA-
USB DATA+	5	6	USB DATA+
GND	7	8	GND
NC	9	10	(null)

2.11 LAN

The board features two RJ45 LAN interfaces, powered by two high-speed network controllers.

- LAN1: Realtek® RTL8125BG – Supports up to 2.5 GbE
- LAN2: Realtek® RTL8111H – Supports up to 1.0 GbE

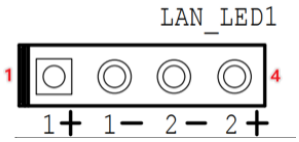
Both LAN1 and LAN2 support Wake-on-LAN (Magic Packet Wake-Up). LAN1 supports UEFI PXE network boot additionally. To enable UEFI PXE boot, please enter the BIOS setup and set IPv4 PXE Support to Enabled.

LED Status Indicators:

LI_LED Status (Green)	Function	ACT_LED Status	Function
Always on	Network	Flashing	Data transmission

LAN_LED Pin definition (Labeled LAN_LED1 onboard)**:**

Singal	LAN1_LED+	LAN1_LED+	LAN2_LED-	LAN2_LED+
Silkscreen	1+	1-	2-	2+
Pin	1	2	3	4

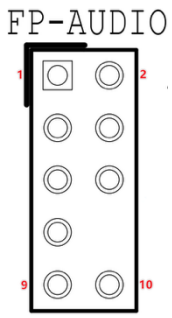


2.12 Audio Interface

The motherboard features a Realtek ALC897 audio codec with rear audio ports, where the green port serves as the Line-out (audio output) and the pink port serves as the Mic-in (microphone input).

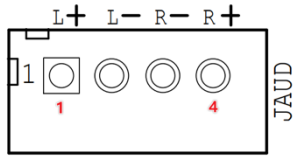
It also provides a front audio header (labeled FP_AUDIO onboard, 2.54 mm pitch), with the JAUD header supporting amplified output.

Front Audio Pin Definition (labeled FP-AUDIO onboard):



Singal	Pin		Singal
MIC2-L	1	2	AGND
MIC2-R	3	4	AVCC（NC）
FRO-R	5	6	MIC2-JD
F-IO-SEN(AGND)	7	8	(N/A)
FRO-L	9	10	LIN2-JD

JAUD (labeled JAUD onboard):

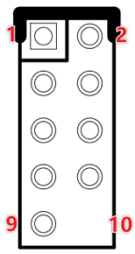


Pin	Singal
1	L+
2	L-
3	R-
4	R+

2.13 COM (labeled COM1, COM2, COM36 onboard)

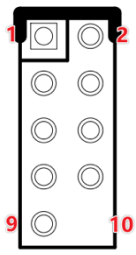
The board features six serial ports, RS232 mode by default. (COM1 and COM2 pins: 2.54mm pitch, COM3-6 pins:2.0mm pitch). COM2 can configured as RS485 mode optionally by hardware components replacing.

COM1 Pin Definition (labeled COM1 onboard):



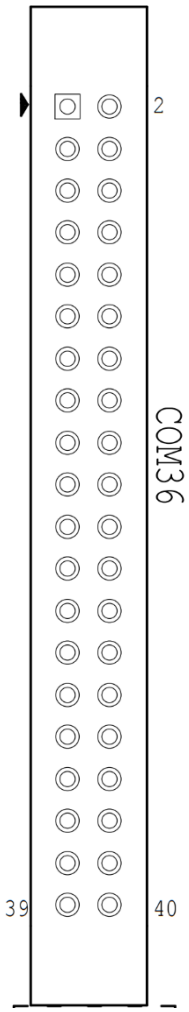
Singal	Pin		Singal
DCD#	1	2	RXD
TXD	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS#
RI#	9		

COM2 Pin Definition (labeled COM1 onboard):



Pin	RS232	RS485
1	DCD#	DATA-
2	RXD	DATA+
3	TXD	(NC)
4	DTR#	(NC)
5	GND	GND
6	DSR#	(NC)
7	RTS#	(NC)
8	CTS#	(NC)
9	RI#	(NC)

COM36 Pin Definition (labeled COM36 onboard):



Singal	Pin		Singal
DCD#	1	2	RXD
TXD	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS#
RI#	9	10	(NC)
DCD#	11	12	RXD
TXD	13	14	DTR#
GND	15	16	DSR#
RTS#	17	18	CTS#
RI#	19	20	(NC)
DCD#	21	22	RXD
TXD	23	24	DTR#
GND	25	26	DSR#
RTS#	27	28	CTS#
RI#	29	30	(NC)
DCD#	31	32	RXD
TXD	33	34	DTR#
GND	35	36	DSR#
RTS#	37	38	CTS#
RI#	39	40	(NC)

2.14 Expansion Slots (labeled M.2-E, PCIEX4 onboard)

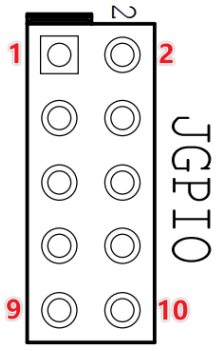
The board features 1x M.2 Key E slot (labeled M.2_E onboard) for 2230 Wi-Fi and Bluetooth Modules (supports PCIe/USB2.0).

1x PCI-E x4 slot (labeled PCIEX4 onboard) for network cards and other PCI-E devices.

2.15 GPIO (labeled JGPIO onboard)

The board features a 2×5-pin JGPIO header (2.0mm pitch), providing 8 programmable input/output ports (see Appendix for GPIO Setting).

GPIO Pin Definition:

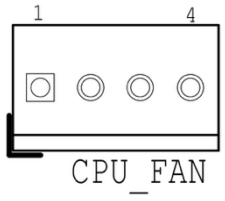


Singal	Pin		Singal
SIO_GP70	1	2	3.3V
SIO_GP71	3	4	SIO_GP74
SIO_GP72	5	6	SIO_GP75
SIO_GP73	7	8	SIO_GP76
GND	9	10	SIO_GP77

2.16 CPU Fan / System Fan (labeled CPU-FAN, SYS-FAN onboard)

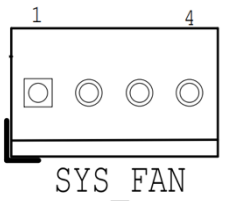
The board features a 4-pin CPU smart fan connector and a 4-pin system fan connector.

CPU Fan Definition (labeled CPU-FAN onboard):



Pin	1	2	3	4
Singal	GND	12V	TAC	CTL

SYSTEM Fan Socket Pin Definition (labeled SYS-FAN onboard)

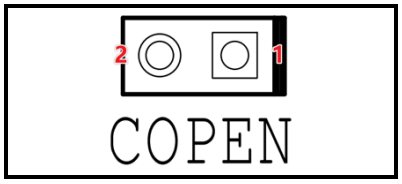


Pin	1	2	3	4
Singal	GND	12V	TAC	CTL

2.17 COPEN Detection Pin (labeled COPEN onboard)

The COPEN pin is used for chassis intrusion detection. By connecting a chassis cover switch to this pin, the system can detect whether the chassis cover has been opened and trigger the corresponding monitoring or protection functions.

Illustration：



Chapter 3 BIOS Setup

3.1 Entering the BIOS

1. Turn on the computer and press <Delete> entering the BIOS
2. BIOS Hotkey Functions:

Key	Function	Description
→←	Select Screen	Navigate between menu screens.
↑↓	Select Item	Move between menu items or options.
Enter	Select	Open a submenu or confirm a selection.
+/-	Change Option	Adjust values or change settings.
F1	General Help	Display help information for the selected item.
F2	Previous Values	Load the previously saved settings.
F9	Optimized Defaults	Restore factory default settings.
F10	Save & Exit	Save changes and exit BIOS.
ESC	Exit	Exit BIOS or return to the previous menu.

3.2 Main Setup (BIOS info, Date, Time）

When you enter the BIOS Setup utility, the first thing you will encounter is the Main Setup screen. Shown below is the Main BIOS Setup screen. You can always return to the Main setup by selecting the Main tab.



BIOS Vendor: American Megatrends

BIOS Version: Displays the current BIOS version

Build Date & Time: Shows the BIOS build date and time

Serial Number: Displays the system or motherboard serial number

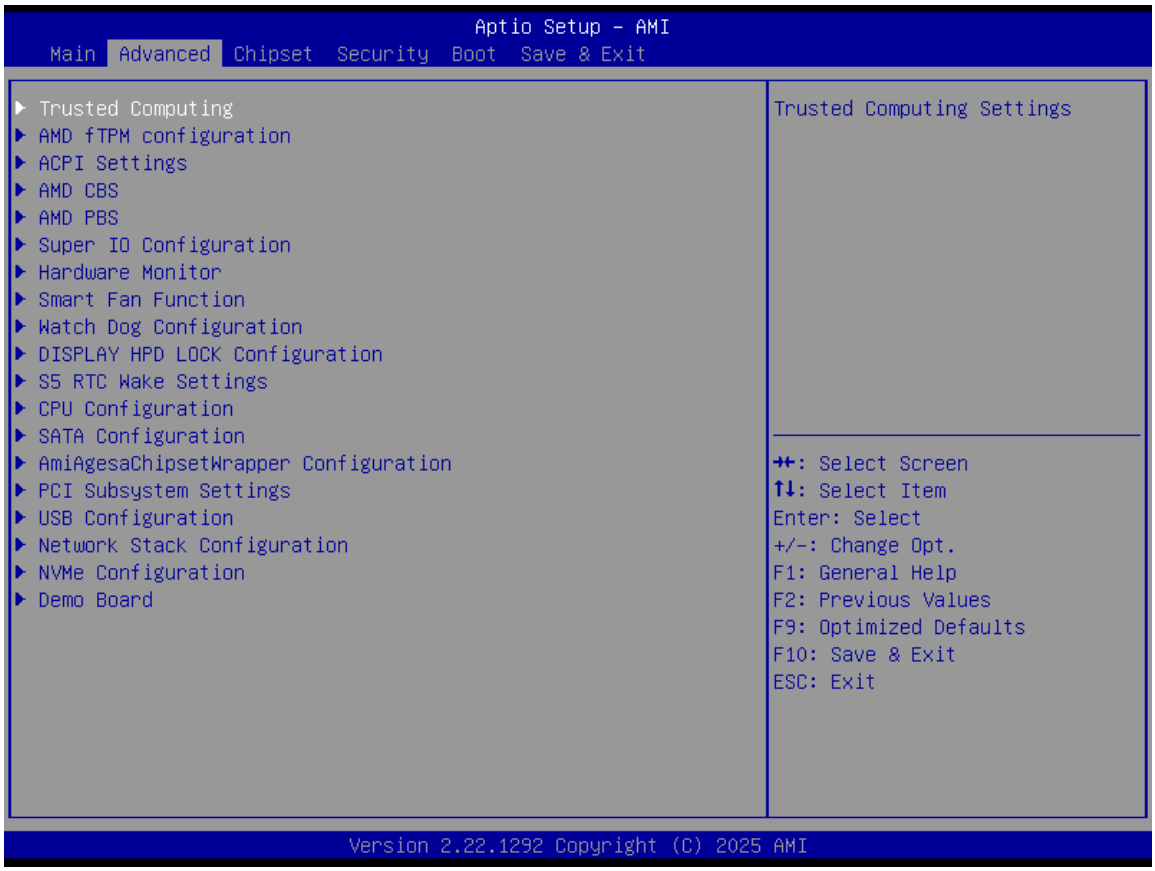
CPU Information: Displays details of the installed CPU

Memory Information: Displays the total installed system memory

System Date: Sets the system date in MM/DD/YYYY format

System Time: Sets the system time in HH:MM:SS (24-hour format)

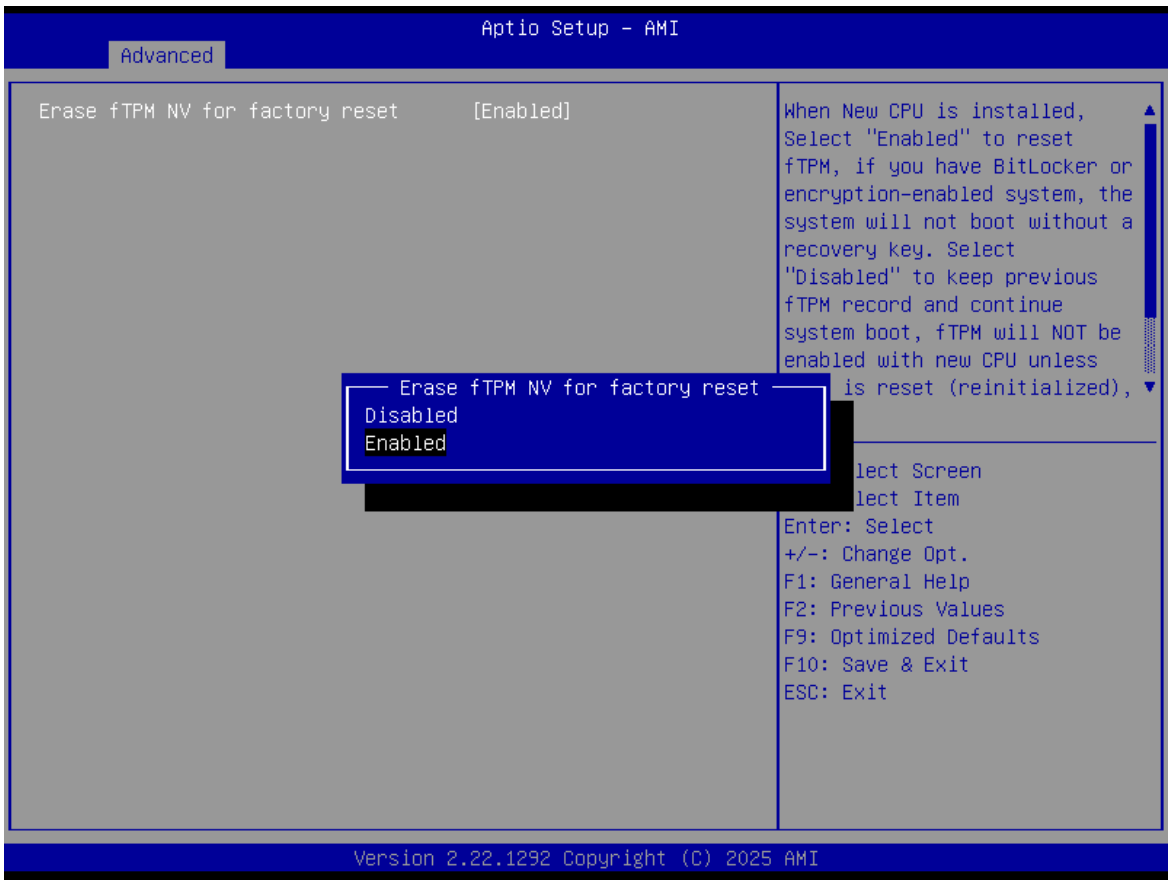
3.3 Advanced Settings



Select any of the items in the left frame of the screen. The advanced sections allow you to configure, improve and set up system features according to the preference of the CPU Configuration. All Advanced BIOS Setup options are described as follows.

- Trusted Computing
- AMD fTPM Configuration
- ACPI Settings
- AMD CBS
- AMD PBS
- Super IO Configuration: Super IO Configuration
- Hardware Monitor
- Watch Dog Configuration
- Display HPD Lock Configuration
- S5 RTC Wake Settings
- CPU Configuration
- SATA Configuration
- AMI Agesa Chipset Wrapper Configuration
- PCI Subsystem Settings
- USB Configuration
- Network Stack Configuration
- NVME Configuration
- Demo Board

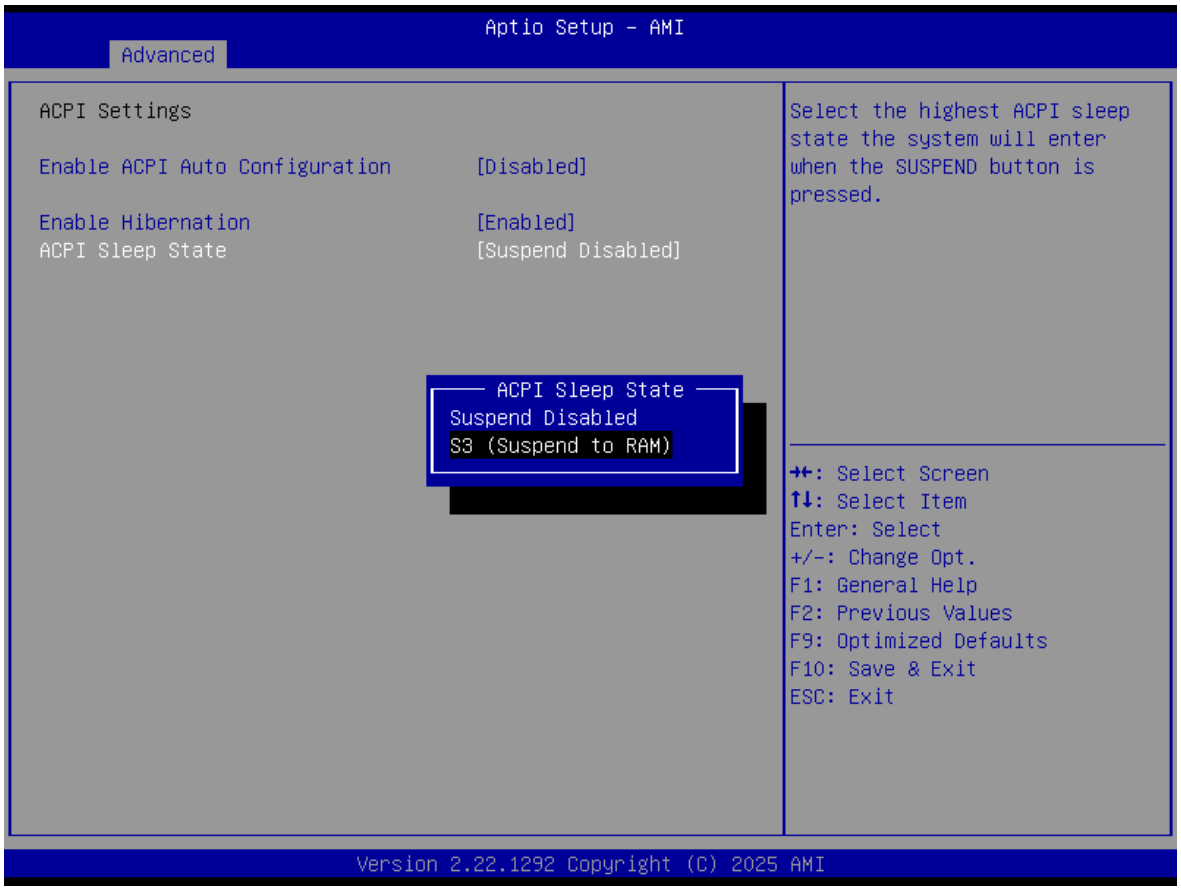
3.3.1 AMD fTPM configuration



AMD fTPM configuration

- Erase fTPM NV for factory reset

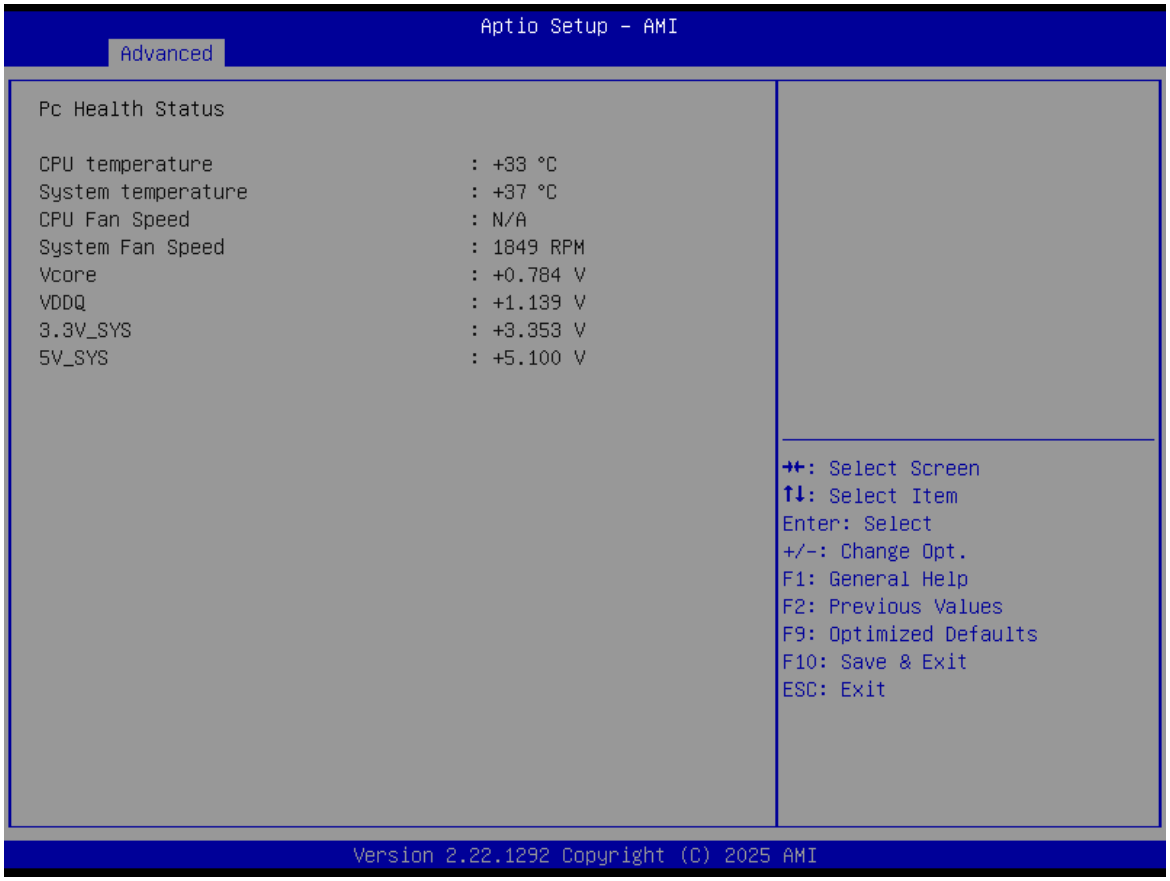
3.3.2 ACPI Settings



ACPI Settings

- Enabled ACPI Auto Configuration
- Enabled Hibernation
- ACPI Sleep State

3.3.3 Hardware Monitor

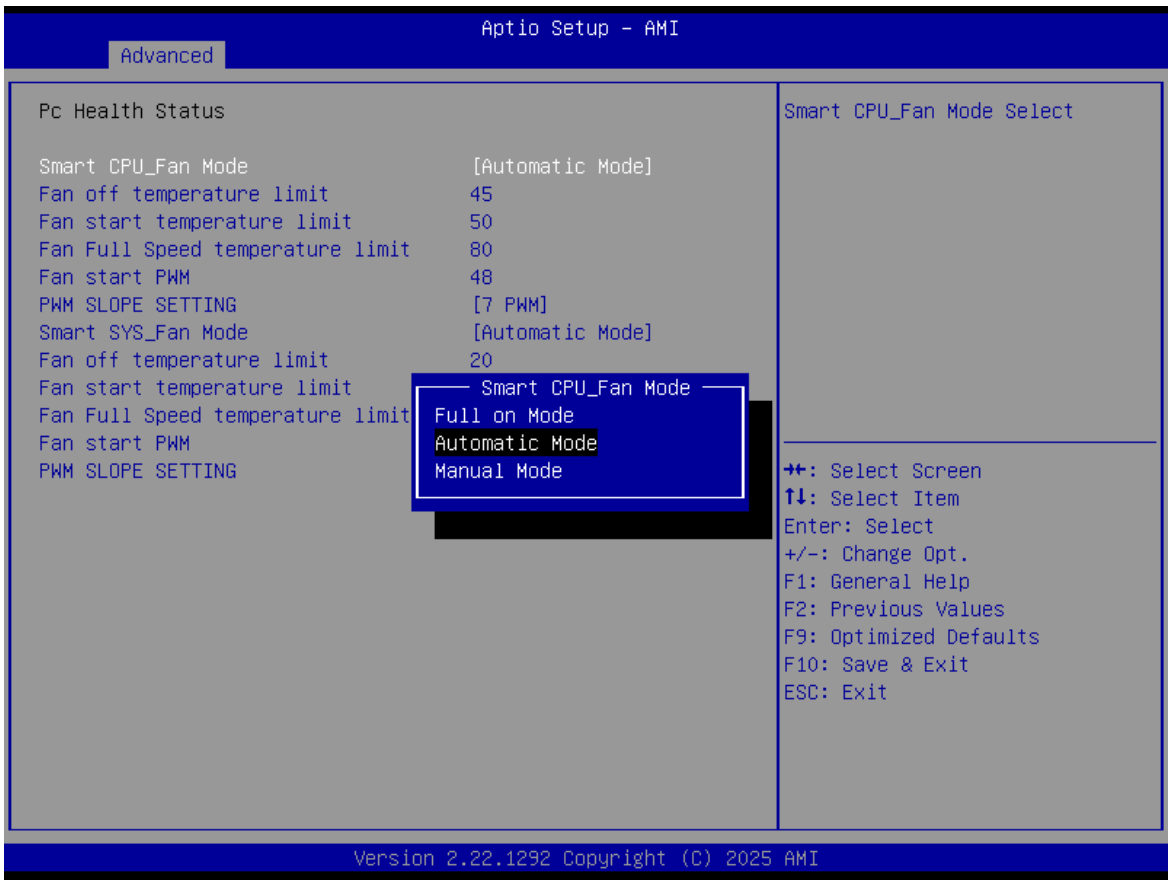


PC Health Status

The PC health status displays CPU temperature, system temperature, fan speed, and other relevant voltage values.

- CPU Temperature
- System Temperature
- CPU Fan Speed
- System Fan Speed
- Vcore: CPU core voltage
- V_DDQ: Memory I/O voltage
- 3.3V_SYS: 3.3V
- 5V_SYS: 5V

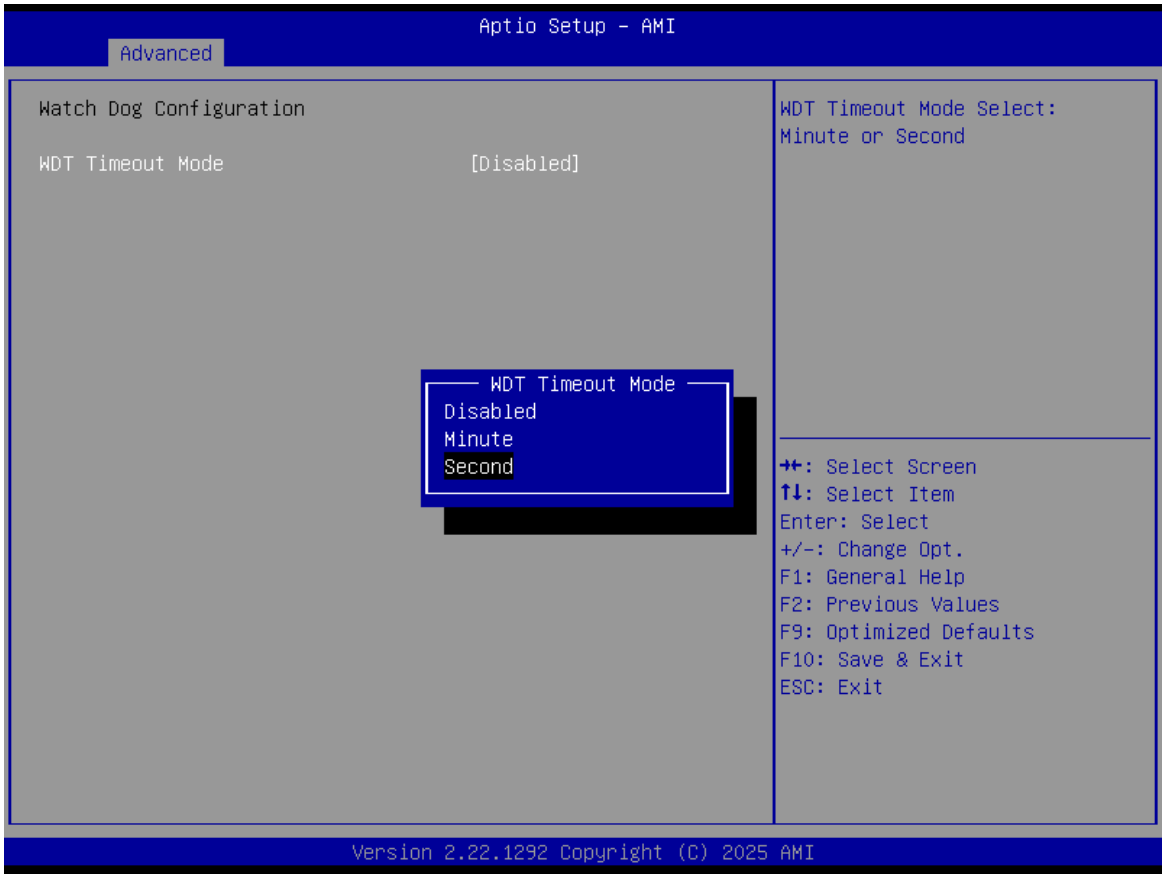
3.3.4 Smart Fan Function



PC Health Status → Smart CPU_Fan Mode

- Smart CPU_Fan Mode/Smart SYS_Fan Mode
- Automatic Mode
- Full on Mode
- Manual Mode
- Fan off temperature limit
- Fan start temperature limit
- Fan Full Speed temperature limit
- Fan start PWM
- PWM SLOPE SETTING

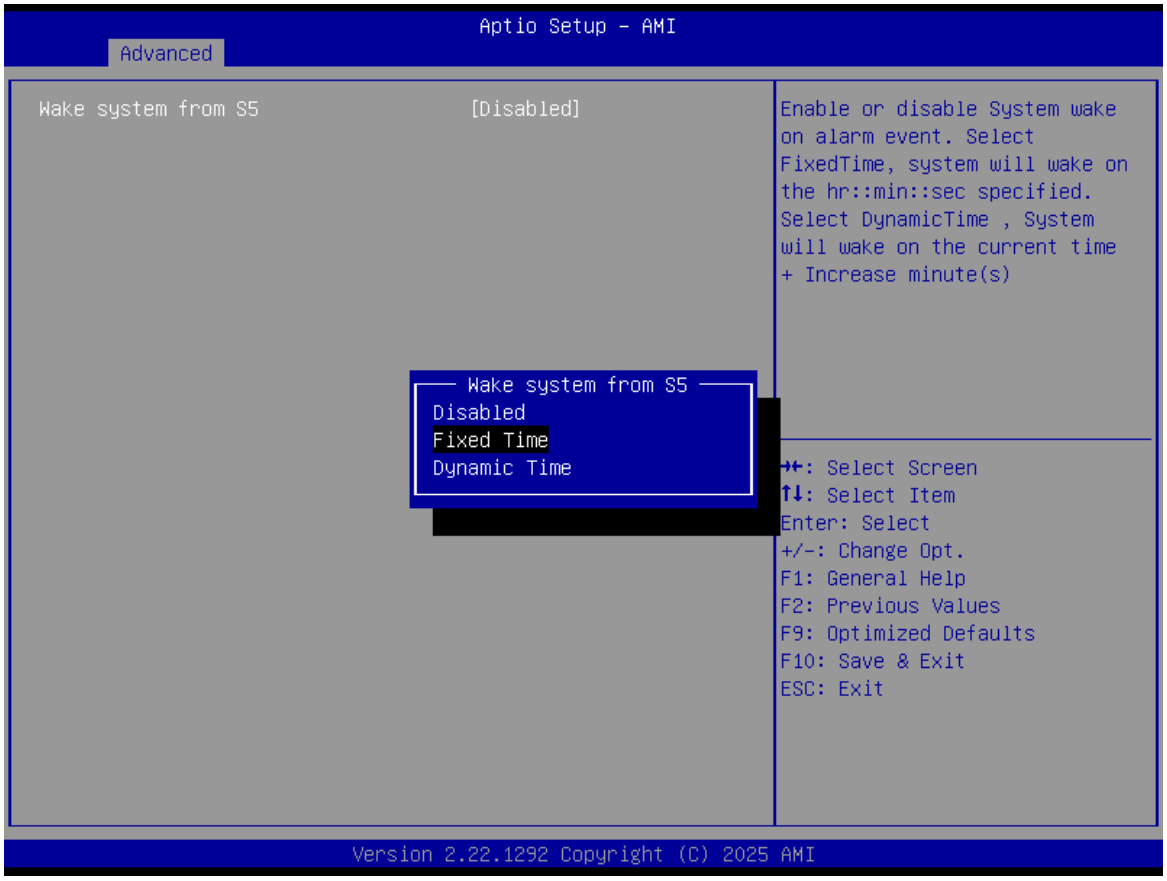
3.3.5 Watch Dog Configuration



Watch Dog Configuration

WDT Timeout Mode: Select Minute or Second

3.3.6 S5 RTC Wake Settings



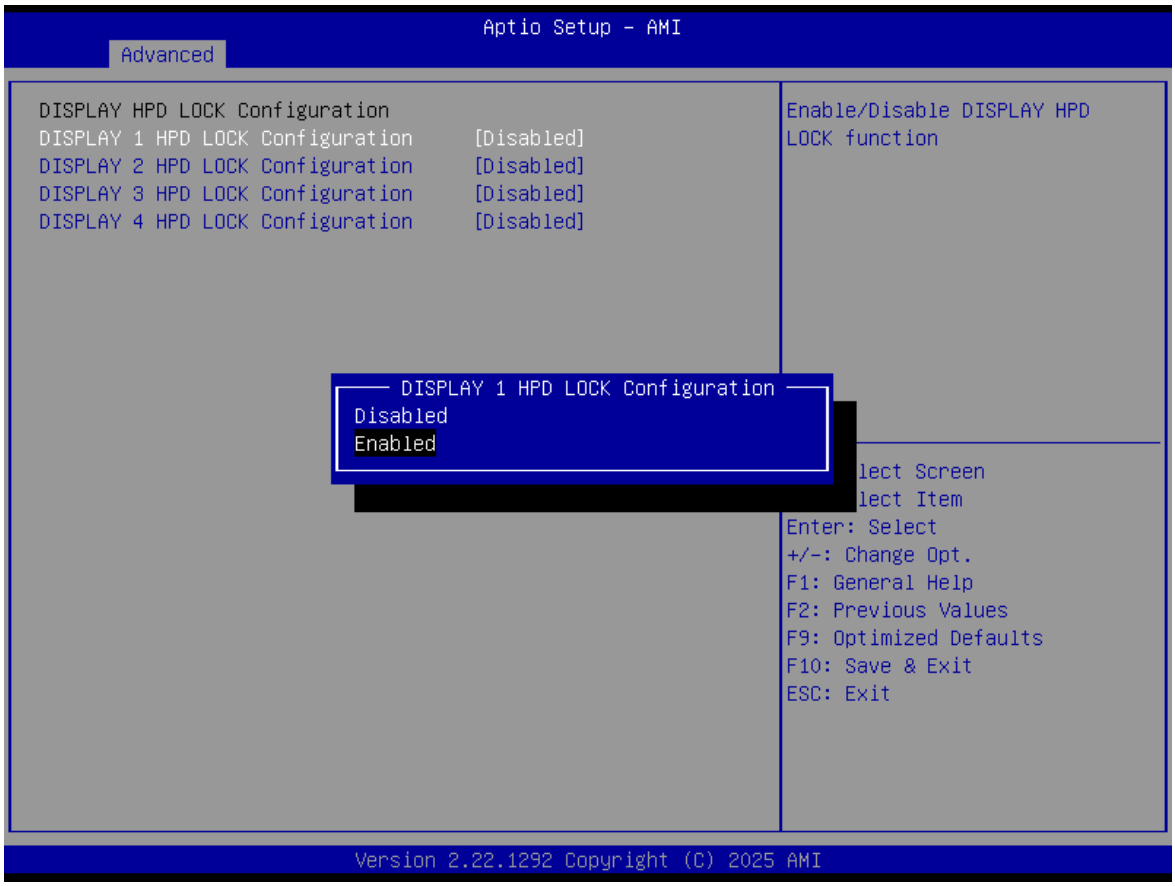
Wake system From S5: timing boot settings, disabled by default.

Fixed Time: Select Fixed Time and the system will wake on the Hr: Min: Sec specified.

Dynamic Time: Select Dynamic Time and the system will wake on a dynamic time.

3.3.7 DISPLAY HPD LOCK Configuration

This option controls the Hot-Plug Detect (HPD) lock function for DisplayPort outputs. Enabling HPD lock stabilizes the display connection by preventing unnecessary link re-training when the monitor power state changes or the cable is reconnected.



DISPLAY HPD LOCK Configuration

- **[Enabled]:** Turns on HPD lock
- **[Disabled]:** Turns off HPD lock

The following settings are available for individual outputs:

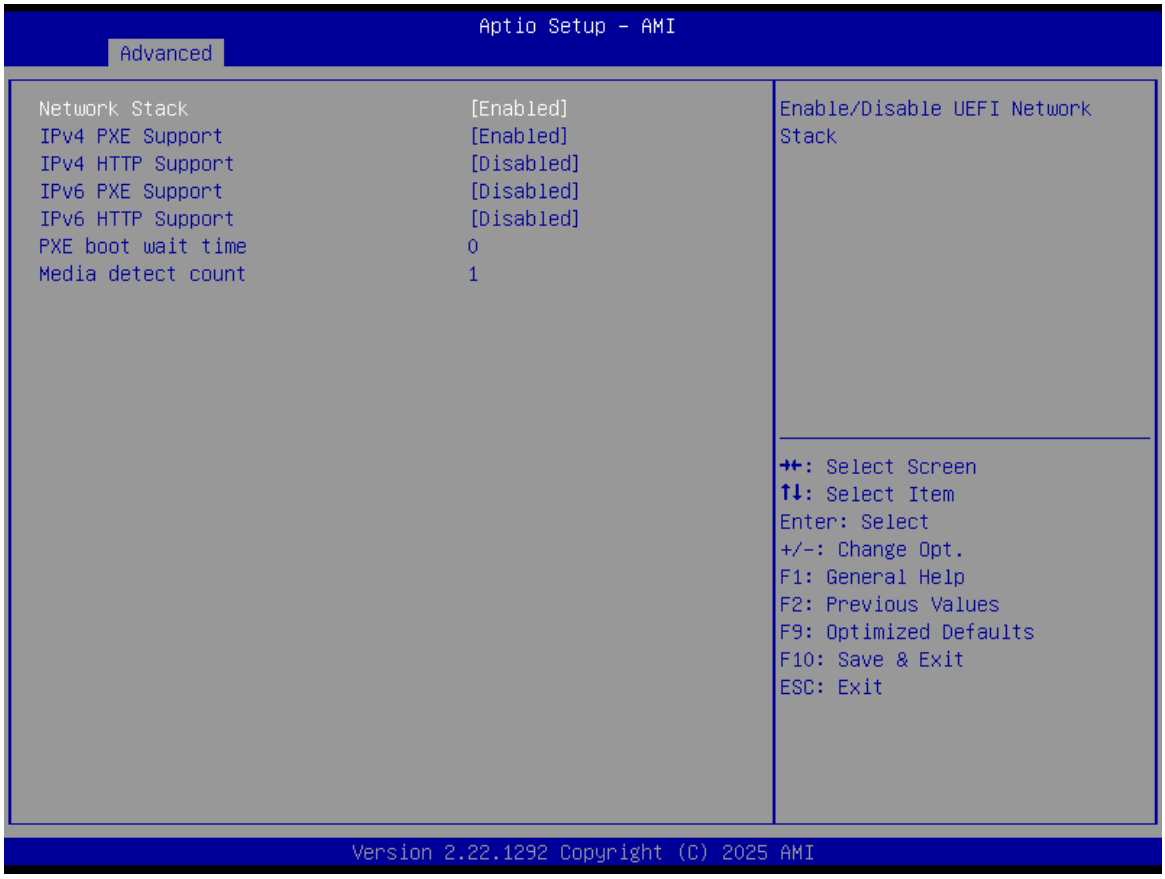
- **DISPLAY 1 HPD LOCK Configuration**
- **DISPLAY 2 HPD LOCK Configuration**
- **DISPLAY 3 HPD LOCK Configuration**
- **DISPLAY 4 HPD LOCK Configuration**

3.3.8 USB Configuration



- **Legacy USB Support**
  - Enable Legacy USB support. Disables legacy support if no USB devices are connected. Select enable will keep USB devices available under UEFI's support.
- **XHCI Hand-off**
  - A workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the USB XCHI driver.
- **USB Mass Storage Driver Support**
  - Enable(default) or disable USB Mass Storage Driver Support.
- **USB transfer time-out**
  - Time-out value for control, bulk, and interrupt transfers, default time:20 second.
- **Device reset time-out**
  - USB mass storage device starts unit command time-out, default time:20 second.
- **Device Power-up Delay**
  - Maximum time the device will take before it properly reports itself to the host controller.

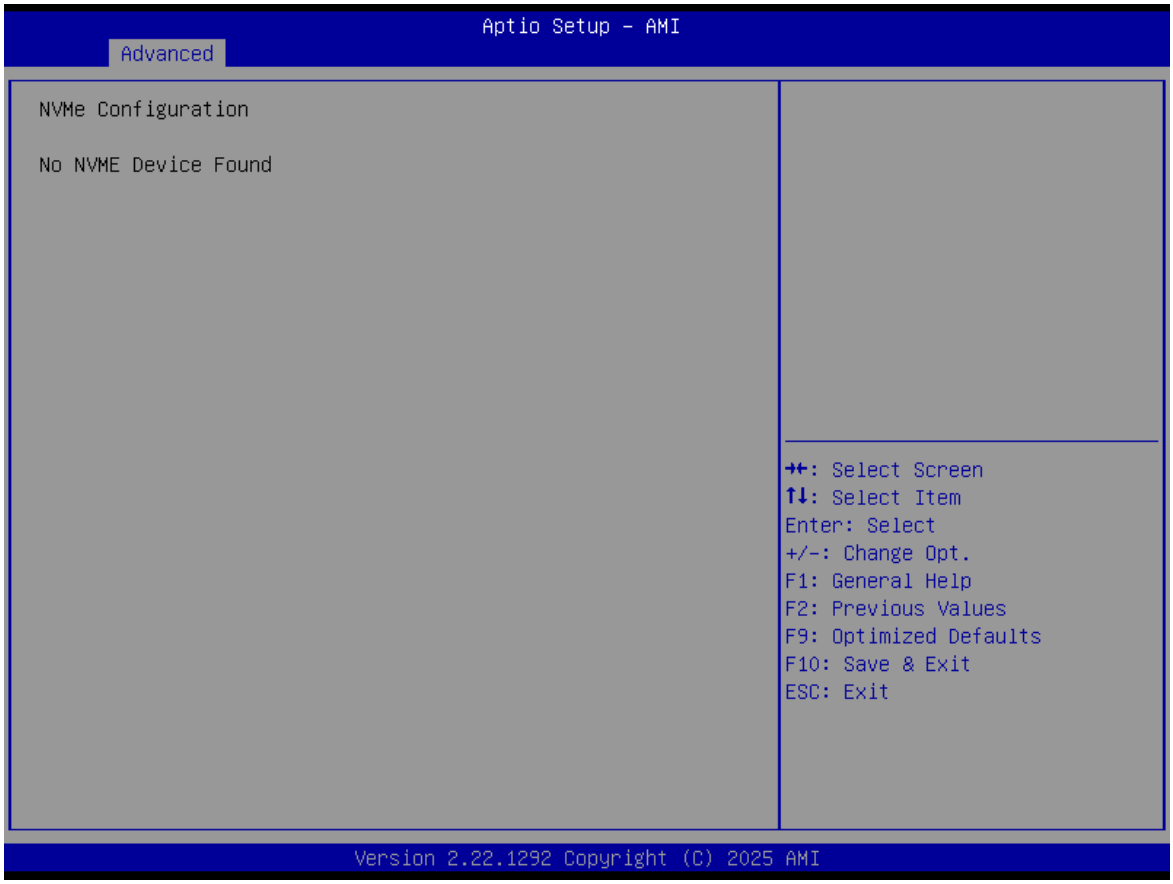
3.3.9 Network Stack Configuration



The Network Stack controls UEFI network boot (PXE/HTTP) and is disabled by default.

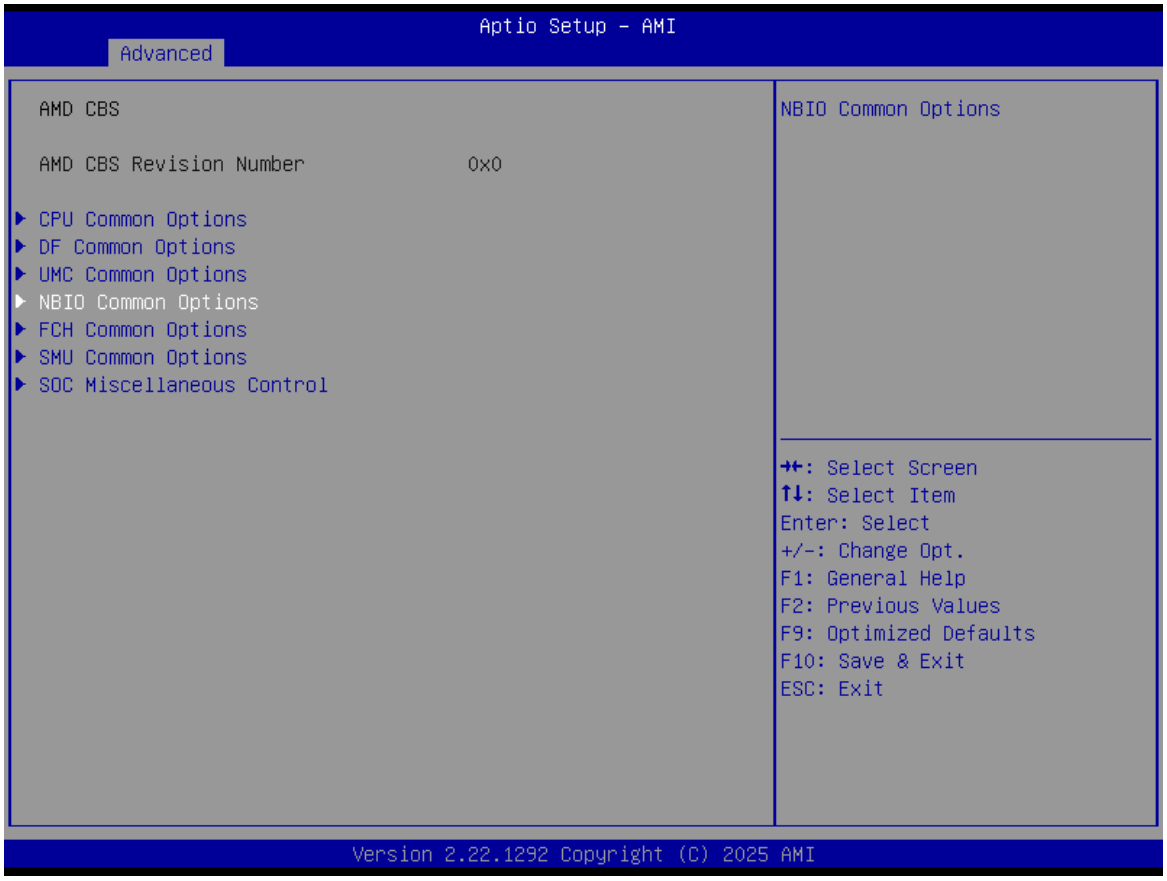
- **IPv4 PXE Support:** PXE boot over IPv4
- **IPv4 HTTP Support:** HTTP boot over IPv4
- **IPv6 PXE Support:** PXE boot over IPv6
- **IPv6 HTTP Support:** HTTP boot over IPv6
- **PXE Boot Wait Time:** Timeout delay for PXE boot
- **Media Detect Count:** Retry count for network device detection

3.3.10 NVME Configuration



The capacity and model of the SSD will be displayed under the option after the NVMe protocol SSD has been installed.

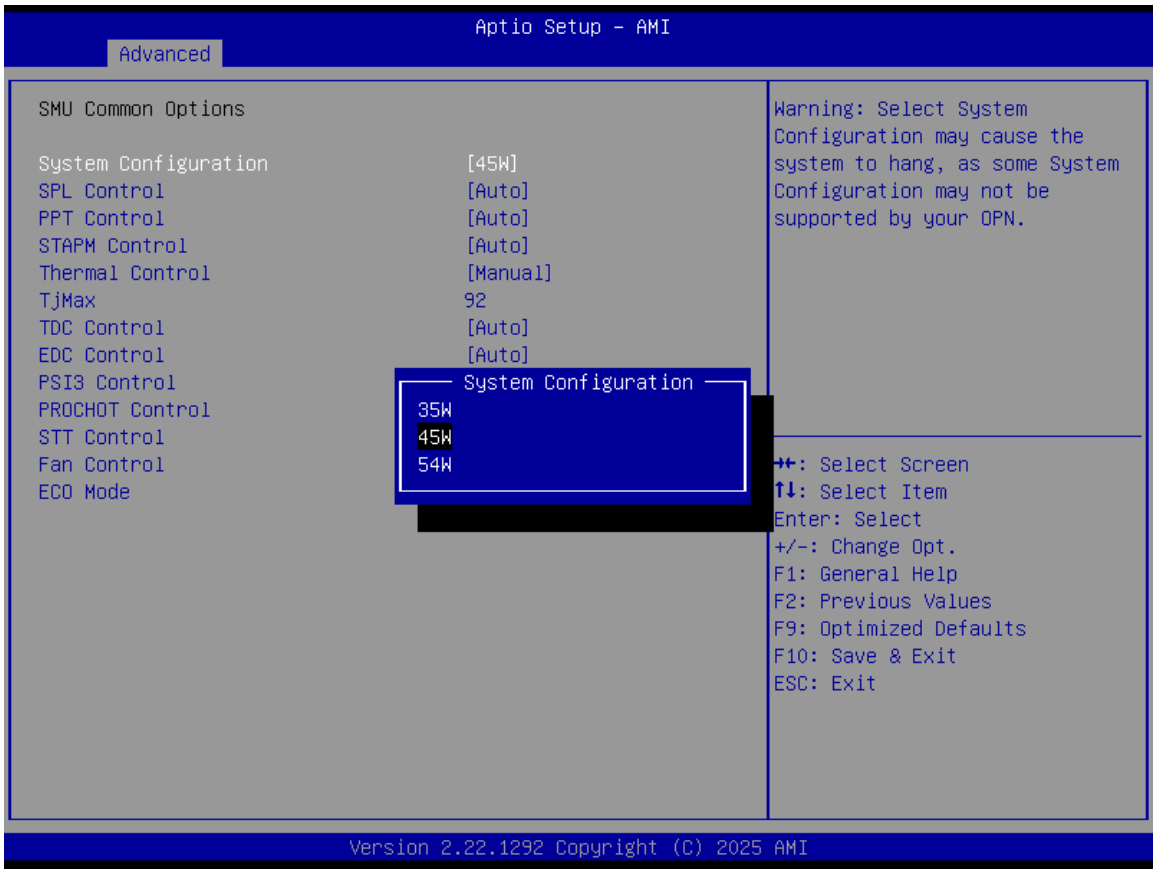
3.3.11 AMD CBS



The AMD CBS (Common BIOS Settings) menu provides access to advanced AMD platform configuration options.

- **AMD CBS Configuration:** Main CBS settings menu
- **CPU Common Options:** CPU configuration options
- **DF Common Options:** Data Fabric configuration options
- **UMC Common Options:** Unified Memory Controller options
- **NBIO Common Options:** Northbridge I/O options
- **FCH Common Options:** Fusion Controller Hub options
- **SMU Common Options:** System Management Unit options
- **SOC Miscellaneous Control:** Miscellaneous SoC settings

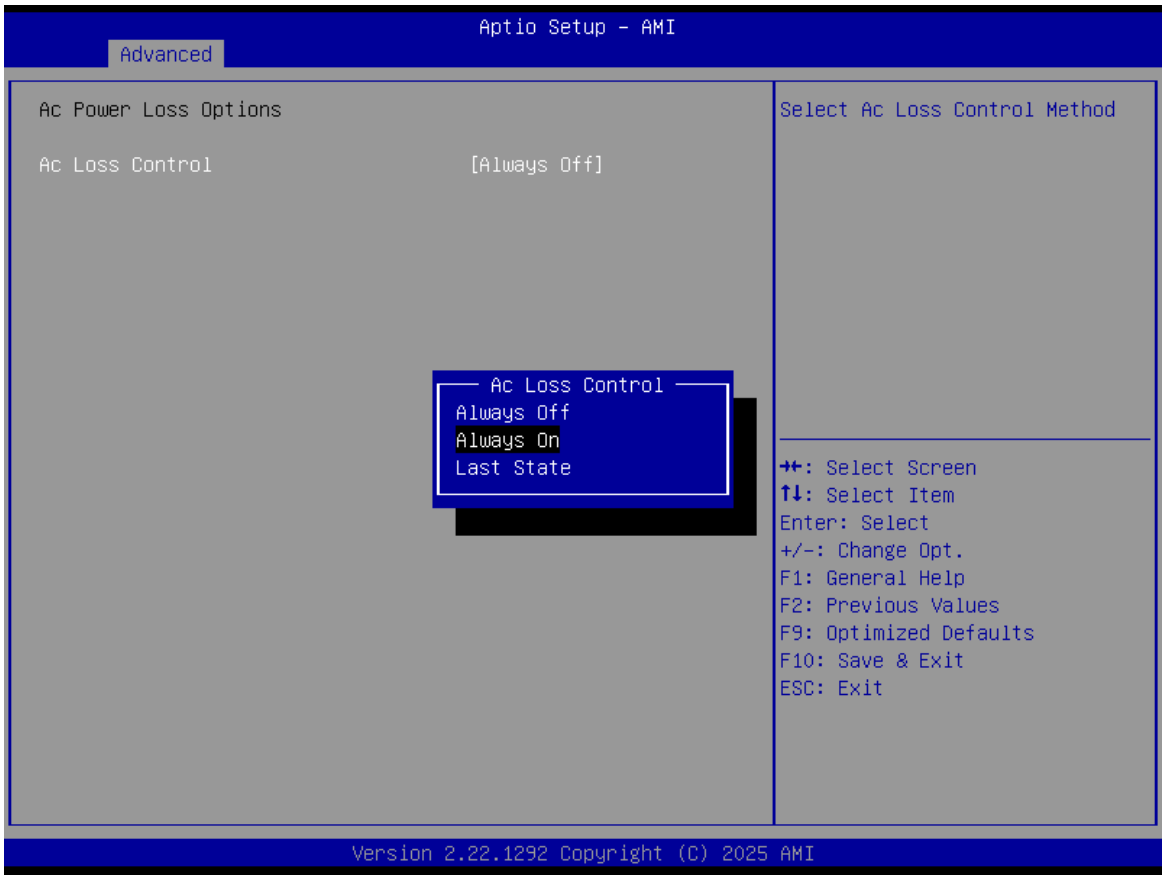
3.3.12 SMU Common Options



SMU Common Options: This menu provides power and thermal management settings controlled by the System Management Unit (SMU).

- System Configuration: Sets the CPU TDP upper limit (default 45W; selectable 35W/55W depending on thermal design)
- SPL Control: Sustained Power Limit (default Auto)
- PPT Control: Package Power Tracking limit (default Auto)
- STAPM Control: Skin Temperature Aware Power Management (default Auto)
- Thermal Control: Thermal management options
- Tjmax: Maximum CPU junction temperature limit
- SOC Miscellaneous Control: Miscellaneous SoC power/thermal settings
- PSI3 Control: Power state interface control
- PROCHOT Control: Processor overheat protection control
- STT Control: Skin Temperature Target control
- Fan Control: System fan configuration
- ECO Mode: Energy-saving mode

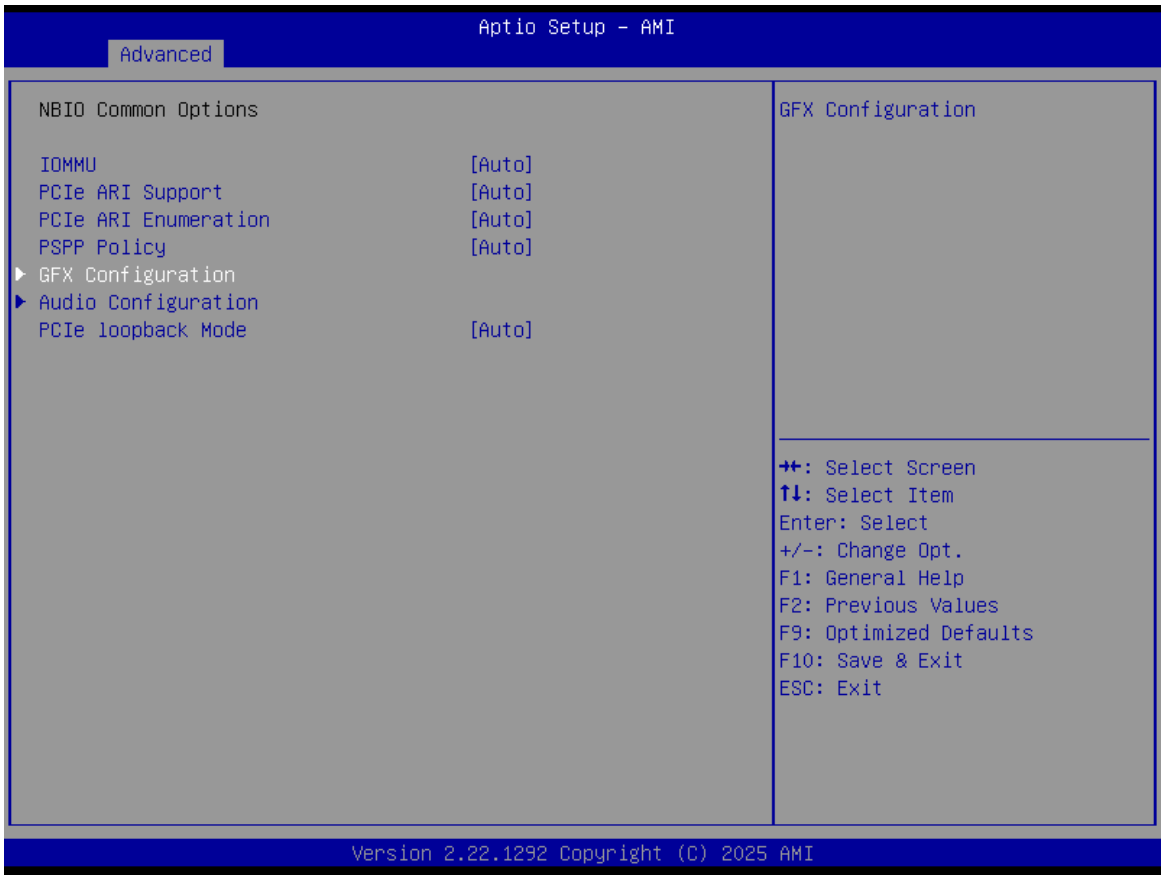
3.3.13 FCH Common Options



Fusion Controller Hub (AMD's southbridge)： This menu controls system behavior after AC power loss.

- **AC Power Loss Options / AC Loss Control**
  - **Always Off (default):** System remains off after power is restored
  - **Always On:** System powers on automatically after power is restored
  - **Last State:** System returns to the state before the power loss (stays off if it was shut down normally, auto-starts if it was powered on before an unexpected loss)

3.3.14 NBIO Common Options



The NBIO (North Bridge I/O) Common Options menu provides configuration for integrated graphics and related features.

GFX Configuration → UMA Frame Buffer Size

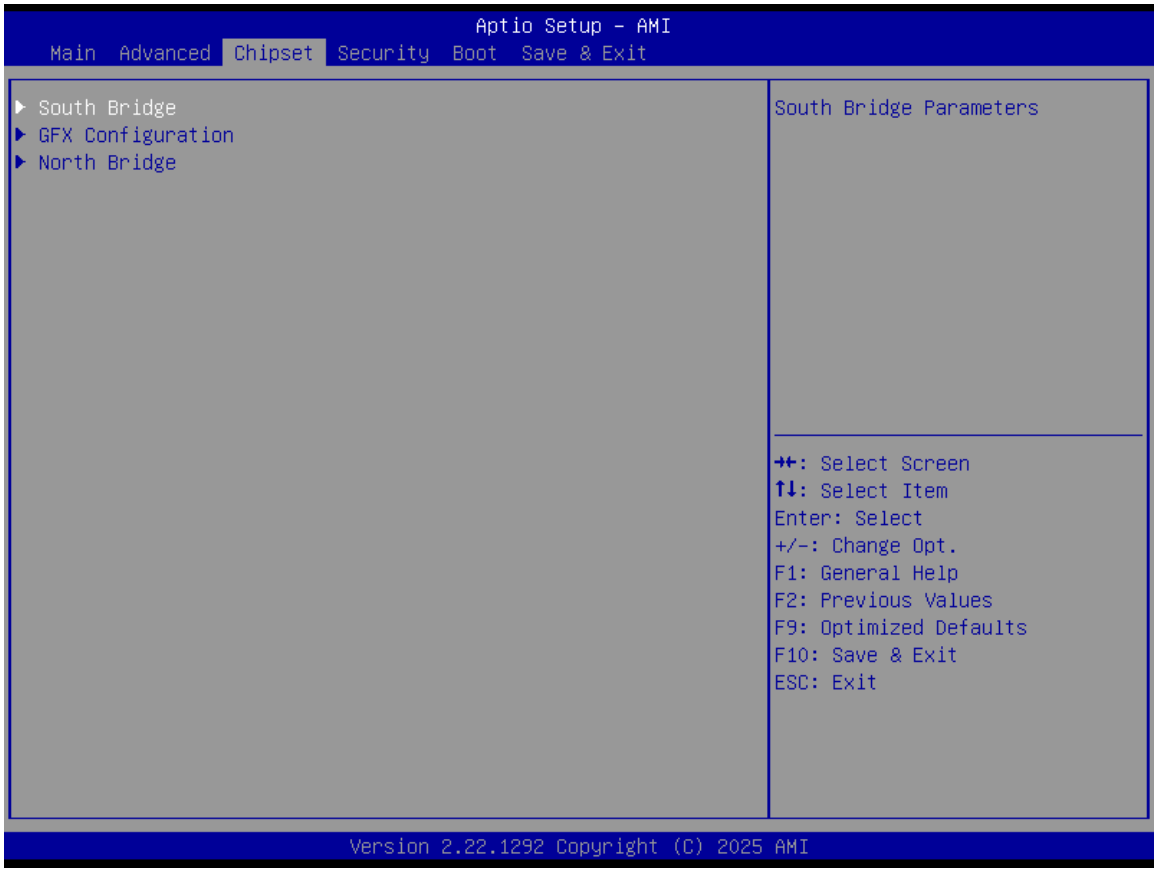
- To adjust the UMA Frame Buffer Size (system memory allocated as video memory for the integrated GPU), enter BIOS by pressing the Delete key during startup when the logo appears. **Navigate to Advanced → AMD CBS → NBIO Common Options → GFX Configuration → UMA Frame Buffer Size.**

The UMA Frame Buffer Size determines how much of the system RAM is reserved for graphics. Increasing this value can improve performance in applications that require more video memory, but it reduces the amount of memory available for the operating system and other applications.

Note!!! Picture for reference only!!! The CPU requires a minimum of 4 GB video memory; increasing this value uses part of system RAM and may reduce stability or performance if set too high, so adjust carefully according to your system's capabilities.

3.4 Chipset

Select the chipset tab from the setup screen to enter the chipset BIOS Setup screen.



Chipset

- South Bridge
- GFX Configuration
- North Bridge

3.5 Security

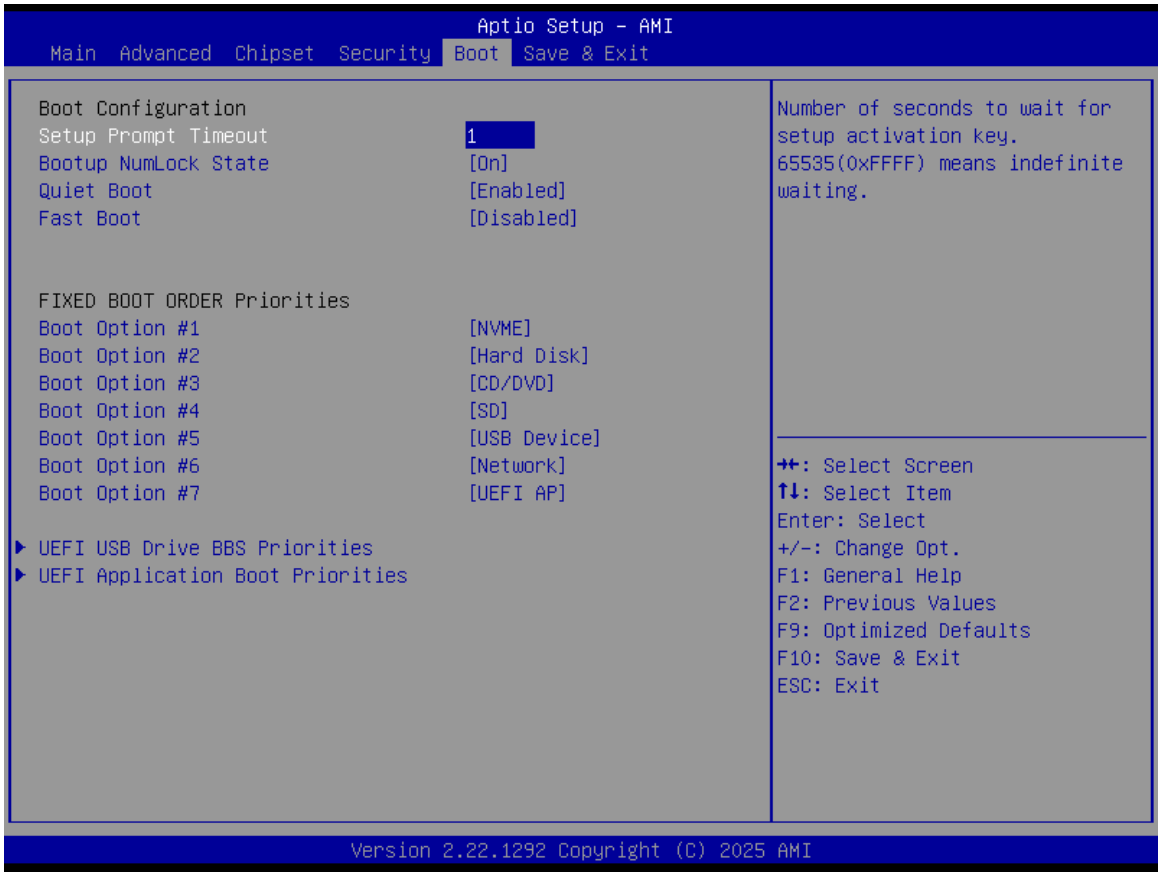


Administrator Password: Set the Administrator Password.

User Password: Set User Password.

Secure Boot: Secure Boot

3.6 BOOT



Setup Prompt Timeout:

Number of seconds that the firmware will wait before initiating the original default boot selection. A value of 0 indicates that the default boot selection is to be initiated immediately on boot. A value of 65535(0xFFFF) indicates that firmware will wait for user input before booting. This means the default boot selection is not automatically started by the firmware.

Bootup NumLock State:

Select the keyboard NumLock State. This option specifies the state of the keyboard NumLock function after the system starts. When set to On (default), the numeric keypad is enabled for number entry immediately after startup. When set to Off, the numeric keypad operates in cursor control mode during startup.

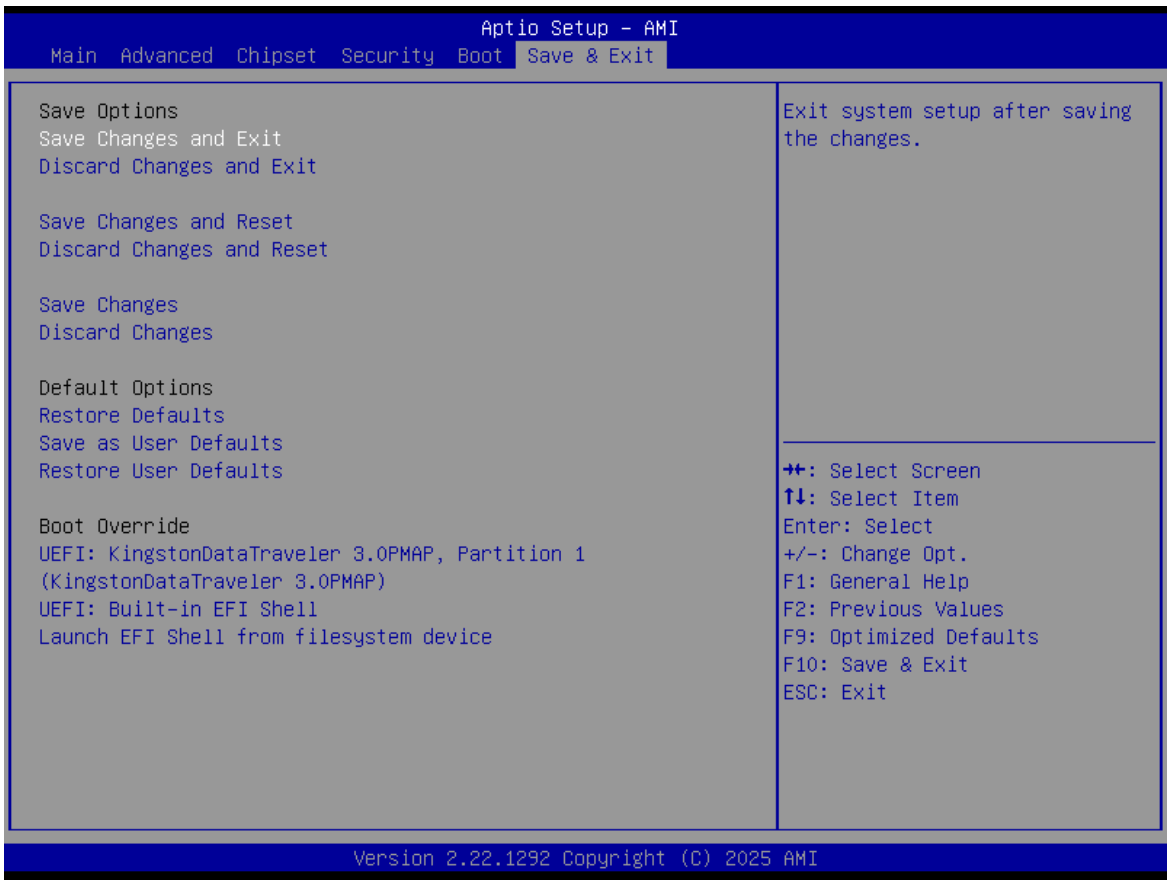
Show Full Logo: Enabled/Disabled Displays customized boot logo.

Boot Option #1~#7: Set the system boot order from Number 1 to Number 7.

UEFI USB Drive BBS Priorities: UEFI USB Drive BBS priorities setting.

UEFI Application boot Priorities: UEFI application boot priority.

3.7 Save & Exit



Save Changes and Exit: Exit the system setup after saving the changes and continue to start the computer.

Discard Changes and Exit: Exit the system setup without saving any changes and continue to start the computer.

Save Changes and Reset: Reset the system after saving the changes.

Discard changes and Reset: Reset the system without saving any changes.

Save Changes: Save changes done so far to any of the options.

Discard Changes: Discard changes done so far to any of the options.

Restore Defaults: Restore/load default values for all the options.

Save as User Defaults: Save the changes done so far as the user defaults.

Restore User Defaults: Restore the user defaults to all the options.

Boot Override: Boot device selection can override your boot priority. Select the specified boot device such as SATA, USB Flash Disk, EFI Shell, PXE, etc., and boot directly. Or press F11 boot by selecting the specified boot device.

Appendix

GPIO Setting

Accessing GPIO70:
Example: Accessing via IO

Set as output:
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x01); //Bit0=1 set as output，bit0=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x01); // When set as output, Bit0 of I/O address 0xA06 = 1 outputs high level, Bit0 = 0 outputs low level

Set as input：
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00); //Bit0=1 Set as output，bit0=0 Set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); //When set as input, Bit0 of I/O address 0xA06 reflects the read state.

Accessing GPIO71:
Example: Accessing via IO

Set as output:
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x02); // Bit1=1 set as output，bit1=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x02); // When set as output, Bit1 of I/O address 0xA06 = 1 outputs high level, Bit1 = 0 outputs low level

Set as input：
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00); // Bit0=1 set as output，bit1=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit1 of I/O address 0xA06 reflects the read state.

Accessing GPIO72:
Example: Accessing via IO

Set as output:
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x04); //Bit2=1 set as output，bit2=0 set as input
WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x04); // When set as output, Bit2 of I/O address 0xA06 = 1 outputs high level, Bit2 = 0 outputs low level

Set as input：
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00); //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit2 of I/O address 0xA06 reflects the read state.

Accessing GPIO73:
Example: Accessing via IO

Set as output：
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x08);　　//Bit3=1 set as output，bit3=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x08); // When set as output, Bit3 of I/O address 0xA06 = 1 outputs high level, Bit3 = 0 outputs low level

Set as input：
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);　　//Bit3=1 set as output，bi3=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =　ReadIo8 (0xA06); // When set as input, Bit3 of I/O address 0xA06 reflects the read state.

Accessing GPIO74:
Example: Accessing via IO

Set as output:
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x10); //Bit4=1 set as output， bit4=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x10); // When set as output, Bit4 of I/O address 0xA06 = 1 outputs high level, Bit4 = 0 outputs low level

Set as input：
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00); //Bit4=1 set as output， bit4=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit4 of I/O address 0xA06 reflects the read state.

Accessing GPIO75:
Example: Accessing via IO

Set as output:
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x20); //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x20); // When set as output, Bit5 of I/O address 0xA06 = 1 outputs high level, Bit5 = 0 outputs low level

Set as input：
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00); //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit5 of I/O address 0xA06 reflects the read state.

Accessing GPIO76:
Example: Accessing via IO

Set as output:
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x40); //Bit6=1 set as output， bit6=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x40); // When set as output, Bit6 of I/O address 0xA06 = 1 outputs high level, Bit6 = 0 outputs low level

Set as input：
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00); //Bit6=1 set as output， bit6=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit6 of I/O address 0xA06 reflects the read state.

Accessing GPIO77:
Example: Accessing via IO

Set as output:
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x80); //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x80); // When set as output, Bit7 of I/O address 0xA06 = 1 outputs high level, Bit7 = 0 outputs low level

Set as input：
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00); //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit7 of I/O address 0xA06 reflects the read state.