User Manual

FP510 V1.0

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FP510 User Manual

(Version 1.0)

Release Notes：		
No.	Description	Date
V1.0	Initial Version	2026/4/9

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Warning

1. Before using the product, carefully read the manual to ensure proper installation and operation.
2. If you are not ready to install any extension card, store it in an anti-static protective bag to prevent damage.
3. To discharge any static electricity, briefly touch a grounded metal object before removing the extension card from the protective bag.
4. Always wear anti-static gloves and handle the card by its edges to avoid damaging sensitive components.
5. Verify that the power supply voltage is correct before connecting the motherboard to the power supply.
6. To prevent electric shock or damage, always turn off the AC power or unplug the power cord before removing or reconfiguring the motherboard or any components.
7. Unplug the AC power cord from the outlet before relocating the motherboard or any components.
8. Ensure all power cords are unplugged before connecting or disconnecting any equipment to avoid electrical hazards.
9. Wait at least 30 seconds after powering off the system before powering it on again to prevent unnecessary wear.
10. If any issues arise during operation, consult a qualified professional for assistance.
11. This product may cause radio interference in certain environments; if necessary, users should take appropriate measures to mitigate such interference.

Contents

Chapter 1 Product Introduction 5

1.1 Brief Introduction 5

1.2 Parameters 6

1.3 Connector Diagram 8

Chapter 2 Hardware 10

2.1 Installations 10

2.2 Jumper Setting 11

2.3 Memory 11

2.4 Board Power Supply (labeled PWR1, PWR2/PWR3, PWR4 onboard) 12

2.5 Front Panel Header (labeled JPOWER onboard) 12

2.6 Hardware Auto Power-On (labeled JAT onboard) 13

2.7 CMOS Clearance/Retention (labeled CLR_CMOS onboard) 13

2.8 Display Interfaces 14

2.8.1 LVDS (optional, labeled EDP/LVDS, LVDS-ADJ, L-ADJ/DIS, L-VCC Onboard) 15

2.8.2 eDP(optional) 17

2.9 Storage Interfaces (labeled as M.2_N, M.2_S/W, and SATA) 19

2.10 Expansion Slots (labeled as M.2_E, PCIEX4) 20

2.11 USB Interfaces (labeled as USB30, USB31, USB21, USB22) 21

2.12 LAN (labeled as LAN1/LAN2) 22

2.13 Audio Interfaces (labeled as FP_AUDIO and JAUD) 23

2.14 Serial Ports (Labeled as COM1/COM2/COM36) 24

2.15 GPIO (Labeled as GPIO) 26

2.16 CPU Fan/System Fan Socket (Labeled as CPU_FAN, SYS_FAN) 26

2.17 LPC Header (labeled as LPC) 27

Chapter 3 BIOS Setup 28

3.1 Entering the BIOS 28

3.2 Main Menu (BIOS Info, Date, Time) 29

3.3 Advanced Settings 30

3.3.1 AMD fTPM configuration 31

3.3.2 ACPI Settings 32

3.3.3 Hardware Monitor 33
3.3.4 Smart Fan Function 34
3.3.5 Watch Dog Configuration 35
3.3.6 S5 RTC Wake Settings 36
3.3.7 LVDS Panel Type 37
3.3.8 HDMI HPD LOCK Configuration 39
3.3.9 USB Configuration 40
3.3.10 Network Stack Configuration 41
3.3.11 CSM Support 42
3.3.12 NVME Configuration 43
3.3.13 SATA Configuration 44
3.3.14 AMD CBS 45
3.3.15 NBIO Common Options 46
3.3.16 FCH Common Options 47
3.4 Chipset 48
3.5 Security 49
3.6 BOOT 50
3.7 Save & Exit 51
Appendix 52
GPIO Setting 52

Chapter 1 Product Introduction

1.1 Brief Introduction

The FP510V1.0 is a Mini-ITX motherboard based on the AMD Ryzen™ Embedded platform.

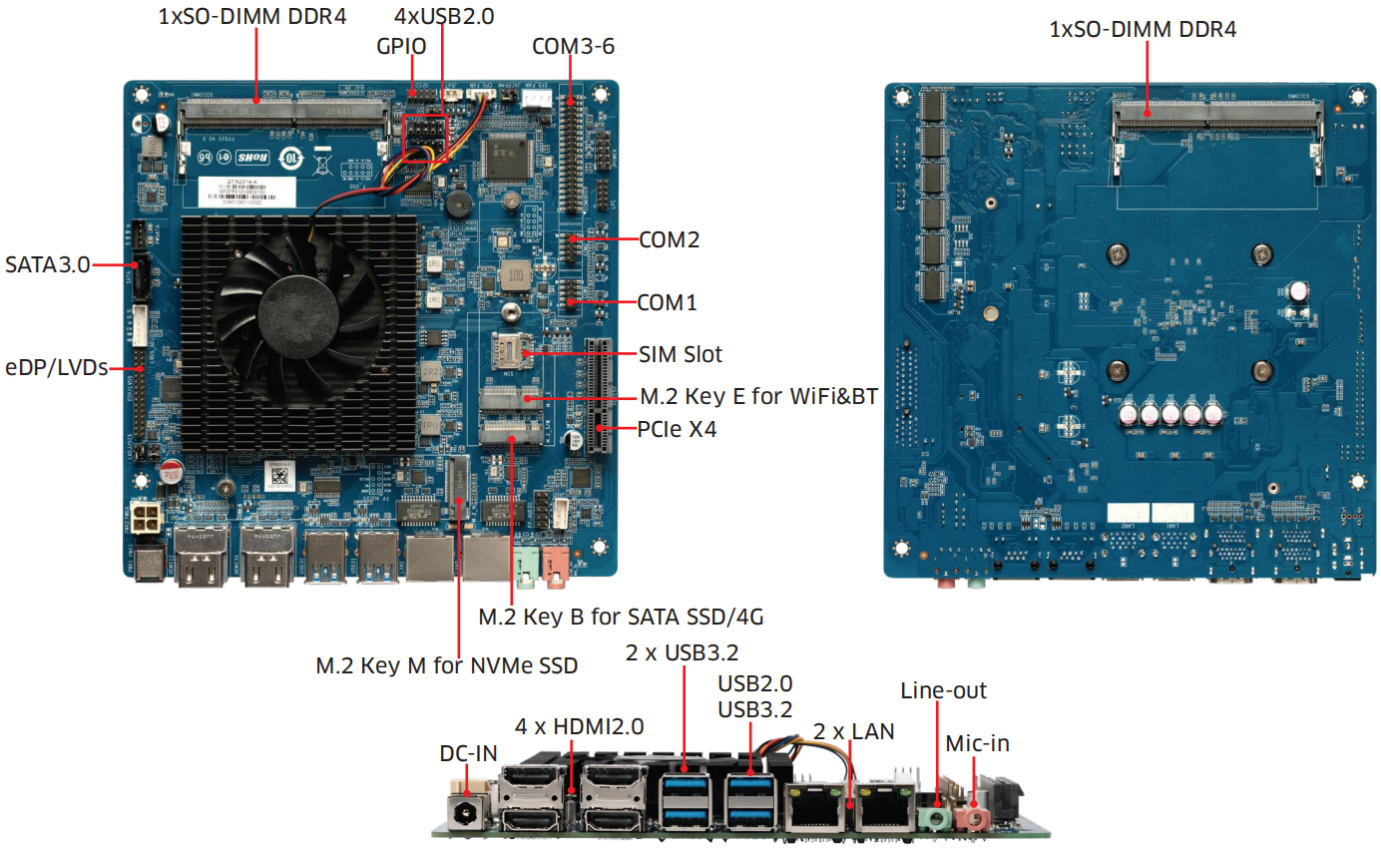


Image for reference only.

1.2 Parameters

CPU: AMD Ryzen™ Embedded R2000 Series

CPU	Cores/Threads	Base Freq.	Max Freq.	Total L3 Cache	Nominal TDP (cTDP Range)
R2314	4C/4T	2.1GHz	3.5GHz	4MB	15W (12-35W)
R2514	4C/8T	2.1GHz	3.5GHz	4MB	15W (12-35W)

GPU: Integrated AMD Radeon™ Graphics with a maximum GPU frequency of up to 1200 Mhz.

Display Interfaces:

- 4 x HDMI2.0
- 1 x LVDS/eDP (labeled as EDP/LVDS on board).

Memory: 2 x DDR4 SO-DIMM slots, dual-channel, up to 64 GB, supporting memory speeds of up to DDR4-2667 MT/s.

Storage/Expansion:

- 1 x M.2 Key M slot (labeled M.2_N on the motherboard), supporting 2280 NVMe SSDs.
- 1 x M.2 Key B slot (labeled M.2_S/W on the motherboard), supporting 2242/2280 SATA SSDs and 3042 4G modules.
- 1 x SATA 3.0 interface (labeled SATA on the motherboard).
- 1 × M.2 Key E slot (labeled M.2_E on the motherboard), supporting 2230 Wi-Fi and Bluetooth modules via PCIe and USB 2.0.
- 1*PCIe x4 slot (labeled PCIEX4 on the motherboard).

Audio: SenaryTech SN6186 High-Definition Audio Codec, support 1 x Line-out, 1 x Mic-in.

Ethernet: 2 x Realtek RTL8111H Controllers, RJ45 interfaces. Date Rate Per Port: 1.0GbEs.

USB:

- 3 x USB 3.2 Gen 2 Type-A ports (labeled USB30/USB31 on the motherboard), supporting data transfer rates of up to 10 Gbps.
- 5 x USB 2.0 ports, supporting data transfer rates of up to 480 Mbps, including:
    - 1 × USB 2.0 Type-A port (labeled USB31 on the motherboard).
    - 4 × USB 2.0 ports via 2.54 mm pin headers (labeled USB21/USB22 on the motherboard).

Serial COM: 6 x COM headers (labeled COM1/COM2 and COM36, 2.0 mm pitch), supporting RS-232 mode by default; COM2 optionally supports RS-485.

GPIO: 1 x 8-bit GPIO header (labeled GPIO, 2.0 mm pitch)

TPM: External TPM module support (Infineon SLB9670, optional).

Buzzer: 1 x onboard buzzer (labeled BUZZ_M)

Other I/O:

- 1 × JPOWER header (labeled as **JPOWER** on the motherboard), 2.54 mm pitch
- 1 × JAT hardware power-on header (labeled as **JAT** on the motherboard), 2.0 mm pitch
- 1 × PWSATA power connector (labeled as **PWSATA** on the motherboard), 2.0 mm pitch
- 1 × Front audio header (labeled as **F_AUDIO** on the motherboard), 2.54 mm pitch

- 1 × Audio amplifier header (labeled as **JAUD** on the motherboard), 2.0 mm pitch
- 1 × 4-pin CPU fan header with 5V/12V selection (labeled as **CPU_FAN** on the motherboard), 1.25 mm pitch. (5V heatsink included by default)
- 1 × 4-pin system fan header with 5V/12V selection (labeled as **SYS_FAN** on the motherboard), 2.54 mm pitch
- 1 × Fan voltage selection header (labeled as **JVCCFAN** on the motherboard), supporting 5V/12V selection, 2.0 mm pitch
- 1 × LVDS/eDP backlight polarity selection header (labeled as **LADJ/DIS** on the motherboard), 2.0 mm pitch
- 1 × LCD power selection header (labeled as **L_VCC** on the motherboard), supporting 3.3V/5V/12V output, 2.0 mm pitch
- 1 × LCD backlight power selection header (labeled as **LVDS_ADJ** on the motherboard), 2.0 mm pitch
- 1 × LPC bus header (labeled as **LPC** on the motherboard), 2.0 mm pitch
- 1 × Clear CMOS header (labeled as **CLR_CMOS** on the motherboard), 2.0 mm pitch
- 1 × CR2032 3V battery socket (labeled as **JBAT** on the motherboard), 1.25 mm pitch
- 1 × Nano SIM card slot (labeled as **SIM** on the motherboard)
- a set of JFP pins (labeled as **JFP** on board) (2.0mm)
- a set of JAT hardware auto-start pins (labeled as **JAT** on board) (2.0mm)
- a set of JAUD amplifier pins (labeled as **JAUD** on board) (2.0mm)
- a set of 5V 4-pin CPU fan pins (labeled as **CPU_FAN** on board)
- a SIM card slot

Power: 12V/19V DC-IN (5.5 mm x 2.5 mm DC jack) or 4-pin ATX power connector

Operating Temperature: -20°C to 60°C

Form Factor: Mini ITX

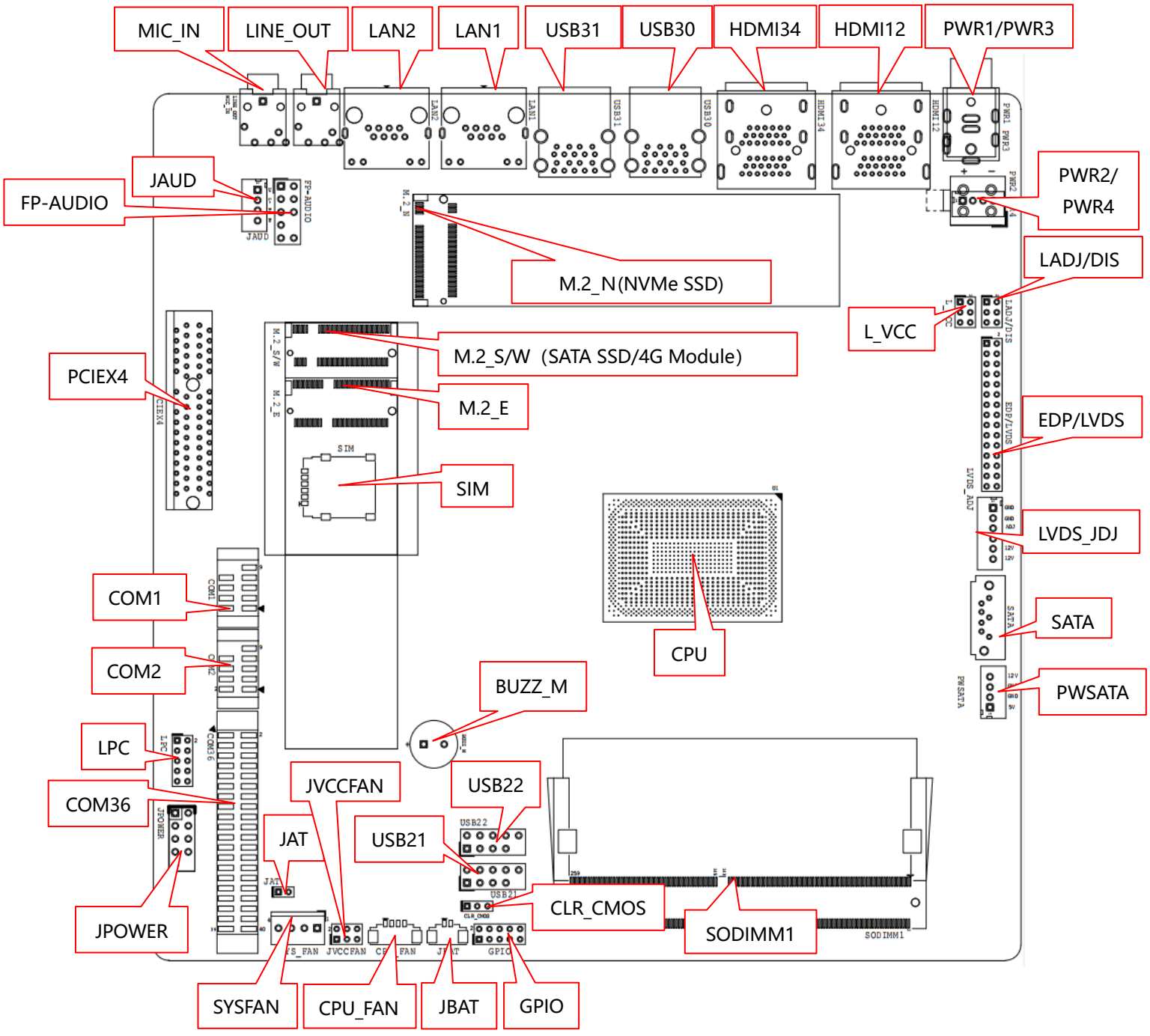
Dimension: 170mm x 170mm

OS Support: Windows 10, Windows 11, and Ubuntu 18.04 or later**.**

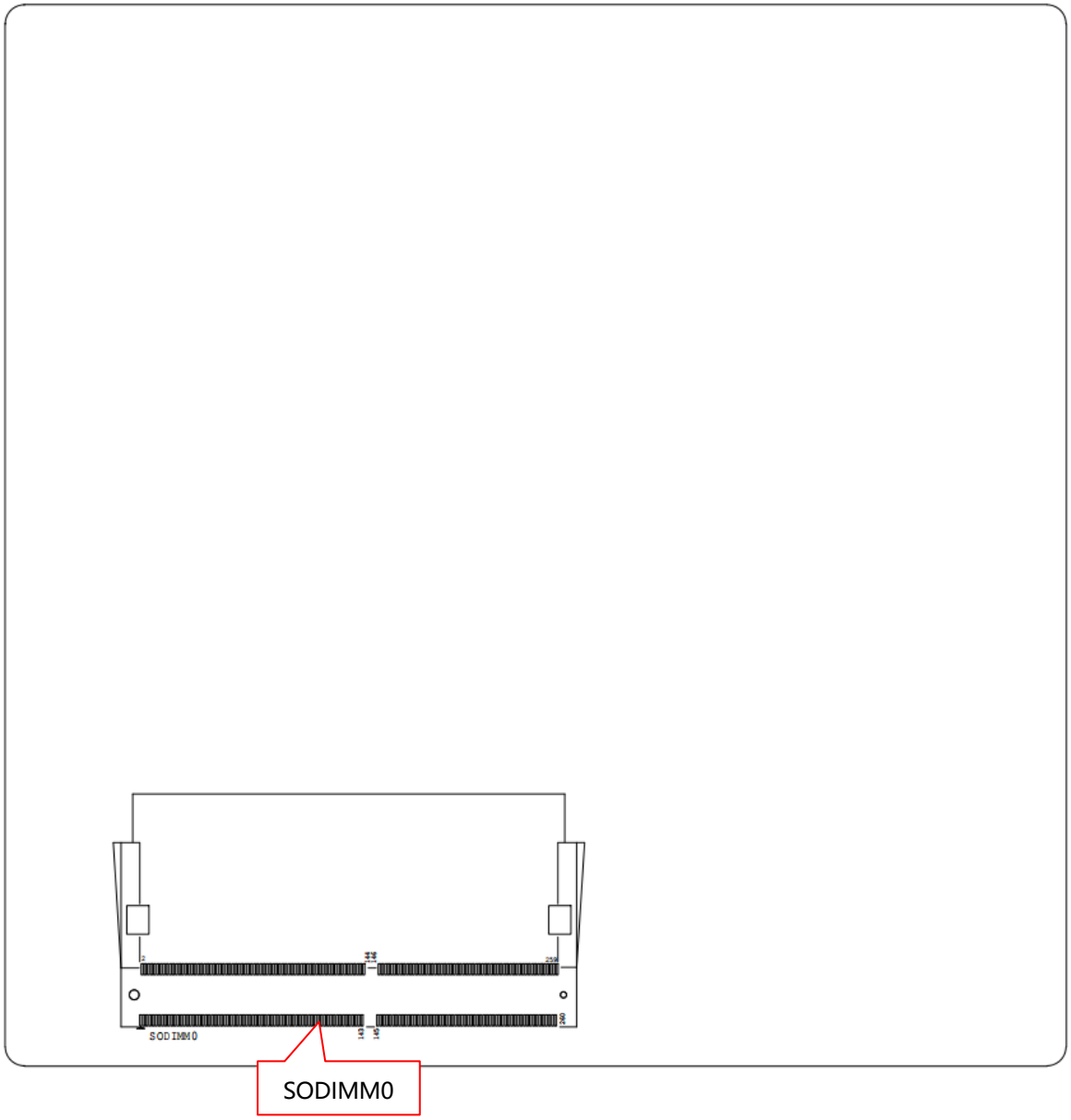
(Please Note: The board does not support Windows 10 version 1703 and earlier or Ubuntu versions earlier than 18.04. Operating system compatibility may vary depending on the installed processor. Please refer to the official documentation from Microsoft and AMD for detailed compatibility information.)

1.3 Connector Diagram

Front:



Back:



Chapter 2 Hardware

2.1 Installations

Please refer to the following steps for installation:

1. Read the user manual carefully to make sure all the adjustments on the FP510 are correct.
2. Installing the Memory:
   - Press the ejector tab of the memory slot outwards with your fingertips.
   - Hold the memory module and align the key to the module with that on the memory slot.
   - Gently push the module into the slot until the ejector levers return completely to the closed position, holding the module in place when the module touches the bottom of the slot. To remove the module, press the ejector levers outwards to unseat the module.
3. Installing the expansion cards:
   - Locate the expansion slots and remove the screw, insert the cards into the slot at a 45-degree angle then attach the screw to the expansion cards, gently press down on it then install the screw back.
4. Connect all signal wires, cables, panel control wiring, and power supplies.
5. Start the computer and complete the setup of the BIOS program.

The board's components are integrated circuits and can easily be damaged by Electrostatic Discharge or ESD; therefore, please follow the instructions:

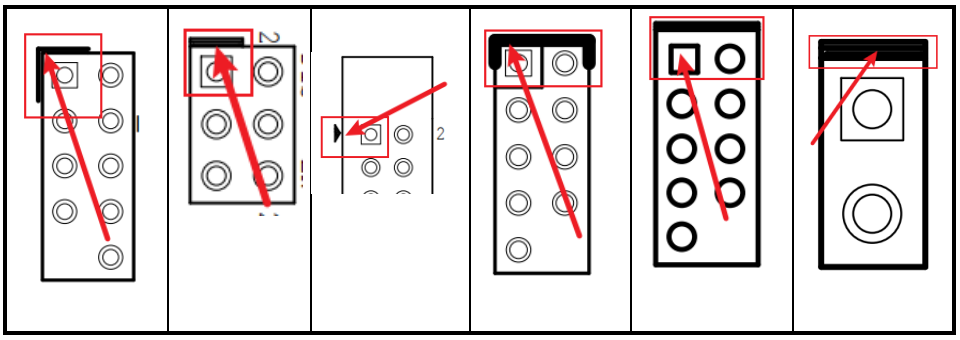
- Hold the board's edge when handing, and do not touch onboard pins, components, or plug sockets.
- When touching integrated circuit components (such as CPU, RAM, etc.), please wear an anti-static wrist strap/glove to avoid electrostatic discharge damage to the board or other sensitive components.
- Before installing the integrated circuits/sensitive components, place the sensitive components in anti-static bags to keep them safe from ESD.
- Please make sure the power switch is OFF before plugging the power plug.

2.2 Jumper Setting

Please configure the jumpers according to your requirements before installing the hardware.

How to identify the first header of jumpers and pins: Observe the mark beside the jumper or pins and find the header marked by “1” or bold line or triangular symbol. Or observe the rear panel and the header with a square solder pad is the first header.

Illustration：



2.3 Memory

The board provides 2x DDR4-2667 MHz SO-DIMM slots, supporting dual-channel with a maximum total capacity of 64 GB.

Ensure the memory module is aligned with the slot key before insertion. When selecting memory, verify that the module meets the required specifications.

Please Note: When using dual-rank (dual-sided) memory modules with a total of 16 memory dies, the AMD Embedded R2314 processor supports a maximum memory frequency of 2400 MT/s. When using dual-rank modules with a total of 8 memory dies, or single-rank (single-sided) modules with a total of 4 memory dies, the maximum supported memory frequency is 2667 MT/s. For additional details, refer to the relevant sections of the AMD processor development documentation.

R2000 MAX DDR4 DATA RATE

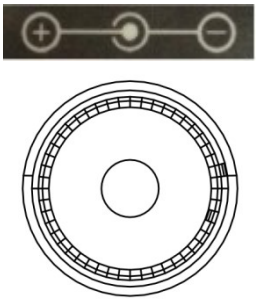
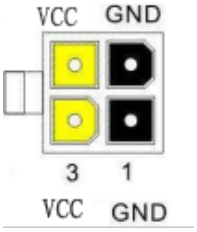
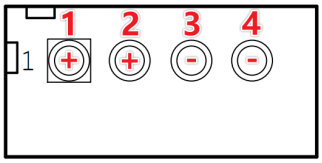
AMD

SO-DIMM OR UDIMM

SoC TDP	Memory Rank	Number of DIMM Socket on Each Channel	Max Data Rate (MT/s)
R2544	Single Rank	1	DDR4-3200
	Dual Rank	1	DDR4-2400
R2314 & R2514	Single Rank	1	DDR4-2667
	Dual Rank	1	DDR4-2400
R2312	Single Rank	1	DDR4-2400
	Dual Rank	1	DDR4-2400

2.4 Board Power Supply (labeled PWR1, PWR2/PWR3, PWR4 onboard)

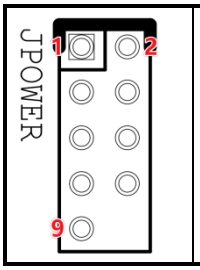
The board supports DC 12V/19V power input via a 5.5 mm × 2.5 mm DC jack (labeled as PWR1 or optional as PWR3 on the motherboard), a 4-pin ATX power connector (labeled as PWR2 on the motherboard, 2 × 2 pin), or an optional PH4 4-pin power connector (labeled as PWR4 on the motherboard, 2.0 mm pitch).

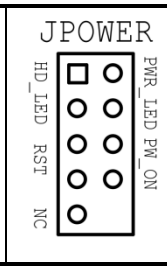
PWR1/PWR3 optional: DC-IN (5.5x2.5mm)	PWR2: ATX Power(2x2PIN)	PWR4 optional: PH4 (4-pin, 2.0 mm)
		

2.5 Front Panel Header (labeled JPOWER onboard)

The JPOWER header is used to connect the chassis front panel switches and status LEDs, including the power button, reset button, power LED, and HDD activity LED.

JPOWER Pin Definition:



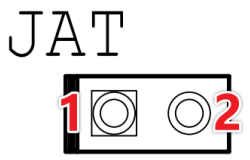


Signal	Pin		Signal
HDD_LED+	1	2	PWR_LED+
HDD_LED-	3	4	PWR_LED-
RSTBTN-	5	6	PWR_ON+
RSTBTN+	7	8	PWR_ON-
NUL	9	10	(Null)

2.6 Hardware Auto Power-On (labeled JAT onboard)

The **JAT** header (labeled **JAT** onboard) controls the hardware power-on auto-start function. Install the appropriate jumper to enable or disable this feature.

JAT Settings:

Enable	Disable
1-2	NC
	

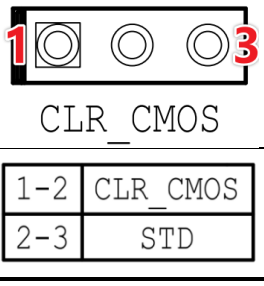
2.7 CMOS Clearance/Retention (labeled CLR_CMOS onboard)

The CMOS memory is powered by the onboard coin-cell battery. Clearing the CMOS will erase all previously saved BIOS settings and restore the BIOS to the factory default configuration.

Steps:

1. Power off the system and disconnect the power supply.
2. Move the jumper cap from pins 2–3 (default) to pins 1–2 for approximately 10 seconds.
3. Return the jumper cap to pins 2–3.
4. Reconnect the power supply and restart the system.

CLR_CMOS: Labeled CLR_CMOS on board.

Clear CMOS	STD
1-2	2-3
	

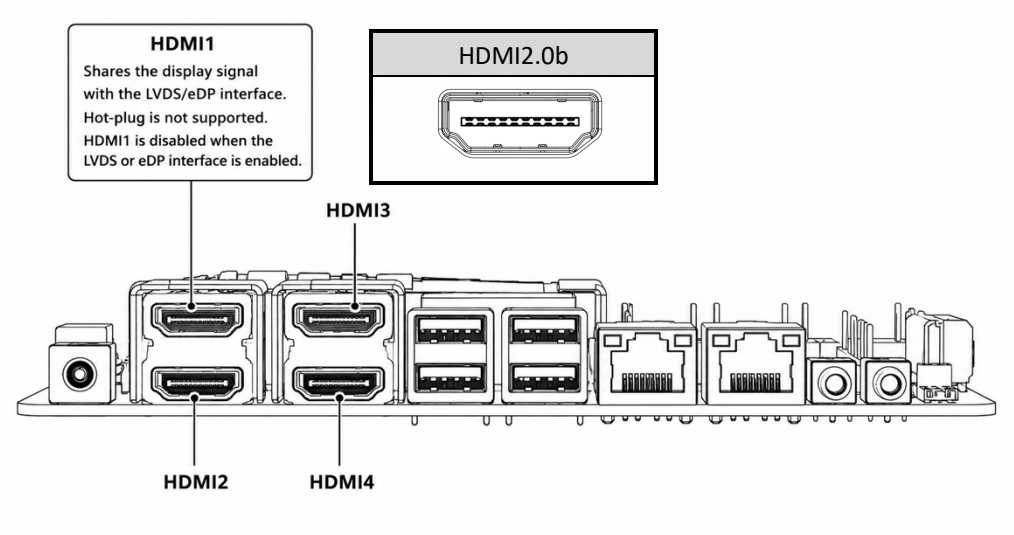
⚠ Caution: Do not clear the CMOS while the system is powered on, as this may damage the motherboard.

2.8 Display Interfaces

The board is equipped with four HDMI 2.0b ports, supporting resolutions up to 4K at 60 Hz. In addition, one optional LVDS or eDP interface is available. The LVDS interface supports a maximum resolution of 1920 × 1200 at 24-bit color depth. The eDP interface supports 3.3V eDP panels with resolutions up to 4K at 30 Hz.

Note: The HDMI1 shares the display signal with the LVDS/eDP interface and does not support hot plug. When the LVDS or eDP interface is enabled, HDMI1 is disabled and no display output is available through this port.

The locations of the display interfaces are shown below.

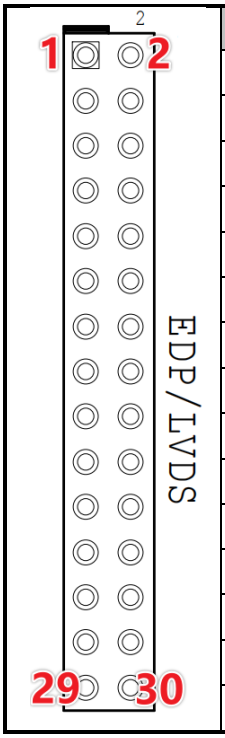


The LVDS/eDP signal is disabled by default. When enabled, the LVDS/eDP display becomes the primary display output, and the BIOS interface is displayed only on the LVDS/eDP screen. During this time, other display outputs (such as HDMI) will not show the BIOS screen. Before connecting an LVDS display, ensure that the panel parameters are configured correctly. If incorrect parameters are applied, the system must be reset by clearing the CMOS before reconfiguring the display settings.

2.8.1 LVDS (optional, labeled EDP/LVDS, LVDS-ADJ, L-ADJ/DIS, L-VCC Onboard)

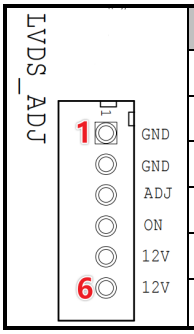
When configured for LVDS mode, the **EDP/LVDS** header outputs LVDS signals. The **LVDS_ADJ** header is used for backlight adjustment, the **LADJ/DIS** header is used for backlight polarity and display signal selection, and the **L_VCC** header is used to configure the LCD operating voltage.

LVDS Pin Definition (labeled as EDP/LVDS)



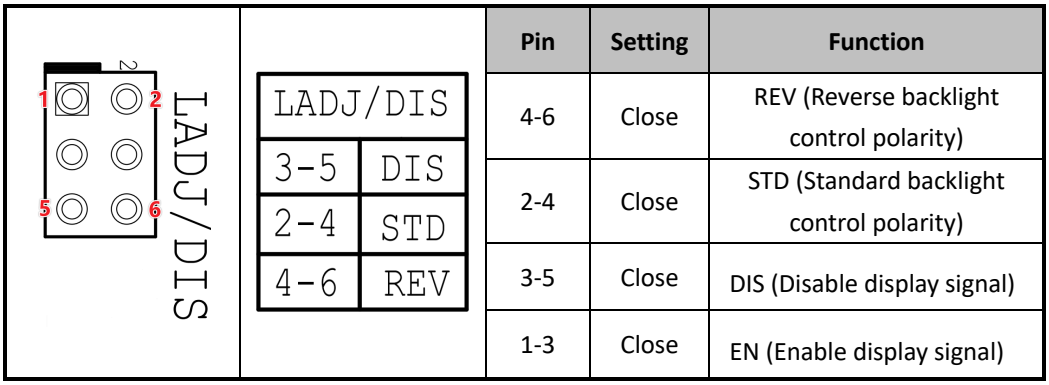
Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	GND
GND	5	6	GND
A_DATA0_DN	7	8	A_DATA0_DP
A_DATA1_DN	9	10	A_DATA1_DP
A_DATA2_DN	11	12	A_DATA2_DP
GND	13	14	GND
A_CLK_DN	15	16	A_CLK_DP
A_DATA3_DN	17	18	A_DATA3_DP
B_DATA0_DN	19	20	B_DATA0_DP
B_DATA1_DN	21	22	B_DATA1_DP
B_DATA2_DN	23	24	B_DATA2_DP
GND	25	26	GND
B_CLK_DN	27	28	B_CLK_DP
B_DATA3_DN	29	30	B_DATA3_DP

LVDS Backlight Header (labeled as LVDS_ADJ onboard)



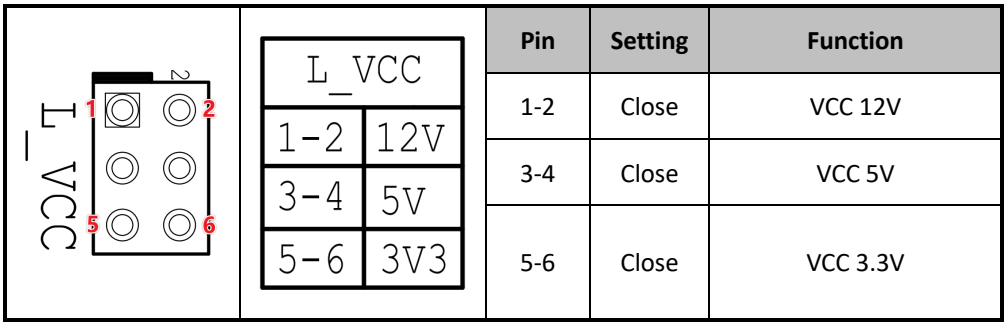
Pin	Signal
1	GND
2	GND
3	LCD_BKL_ADJ
4	LCD_BKL_ON
5	12V
6	12V

LVDS Backlight Polarity / Display Signal Selection Header (labeled as LADJ/DIS onboard)



Pin	Setting	Function
4-6	Close	REV (Reverse backlight control polarity)
2-4	Close	STD (Standard backlight control polarity)
3-5	Close	DIS (Disable display signal)
1-3	Close	EN (Enable display signal)

LVDS Operating Voltage Selection Header (labeled as L_VCC)



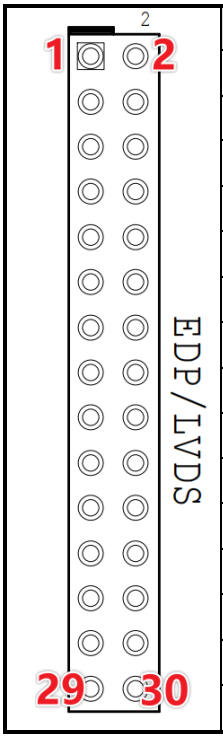
Pin	Setting	Function
1-2	Close	VCC 12V
3-4	Close	VCC 5V
5-6	Close	VCC 3.3V

Note: The LVDS operating voltage is configured using jumper settings. Install a jumper cap on the corresponding pins to select the required output voltage (3.3V, 5V, or 12V) according to the specifications of the connected LVDS panel. ***Do not install jumper caps on multiple voltage settings simultaneously****, as this may damage the display or motherboard.*

2.8.2 eDP(optional)

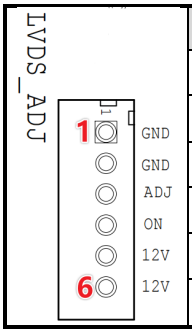
When configured for eDP mode, the EDP/LVDS header outputs eDP signals. The LVDS_ADJ header is used for backlight adjustment, the LADJ/DIS header is used for backlight polarity and display signal selection, and the L_VCC header is used to configure the panel operating voltage.

eDP Pin Definition (labeled as EDP/LVDS)



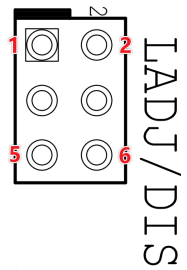
Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	EDP_HPD
GND	5	6	GND
EDP_AUXN	7	8	EDP_AUXP
N/A	9	10	N/A
EDP_DATA0_P	11	12	EDP_DATA0_N
GND	13	14	GND
N/A	15	16	N/A
EDP_DATA1_P	17	18	EDP_DATA1_N
N/A	19	20	N/A
N/A	21	22	N/A
N/A	23	24	N/A
GND	25	26	GND
N/A	27	28	N/A
N/A	29	30	N/A

eDP Backlight Header (labeled as LVDS_ADJ)



Pin	Signal
1	GND
2	GND
3	LCD_BKL_ADJ
4	LCD_BKL_ON
5	12V
6	12V

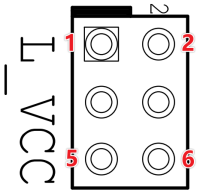
eDP Backlight Polarity / Display Signal Selection Header (labeled as LADJ/DIS)



LADJ/DIS	
3-5	DIS
2-4	STD
4-6	REV

Pin	Setting	Function
~~4-6~~	~~Close~~	~~REV (Reverse backlight control polarity)~~
2-4	Close	~~STD (Standard backlight control polarity~~
~~3-5~~	~~Close~~	~~DIS (Disable display signal)~~
~~1-3~~	~~Close~~	~~EN (Enable display signal)~~

eDP Panel Voltage Selection Header (labeled as L_VCC)



L_VCC	
1-2	12V
3-4	5V
5-6	3V3

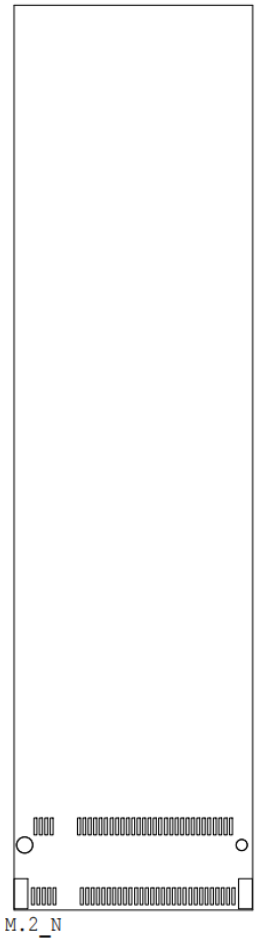
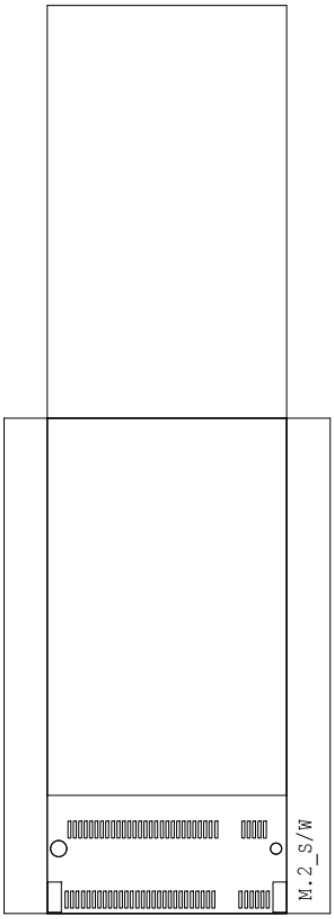
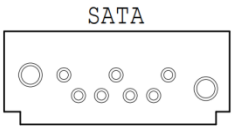
Pin	Setting	Function
~~1-2~~	~~Close~~	~~VCC 12V~~
~~3-4~~	~~Close~~	~~VCC 5V~~
5-6	Close	VCC 3.3V

*Note: The eDP panel voltage is configured using jumper settings. eDP panels support **3.3V only**. Install a jumper cap on pins **5–6** to select **3.3V**. **Do not short multiple voltage settings simultaneously**, as this may damage the motherboard or display panel.*

*Entries shown with strike-through indicate functions or settings that are **unavailable or unsupported** in the current configuration and must not be used or configured.*

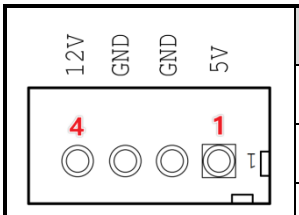
2.9 Storage Interfaces (labeled as M.2_N, M.2_S/W, and SATA)

The board provides one M.2 Key M slot (labeled as M.2_N on the motherboard) with support for 2280 NVMe SSDs. One M.2 Key B slot (labeled as M.2_S/W on the motherboard) is available for 2242 SATA SSDs or 3042 4G modules. The board also features one standard SATA 3.0 connector (labeled as SATA on the motherboard) for SATA storage devices.

M.2_N	M.2_S/W	SATA
		

The board provides one 4-pin PWSATA power header (labeled as **PWSATA** on the motherboard) for SATA device power supply.

PWSATA:



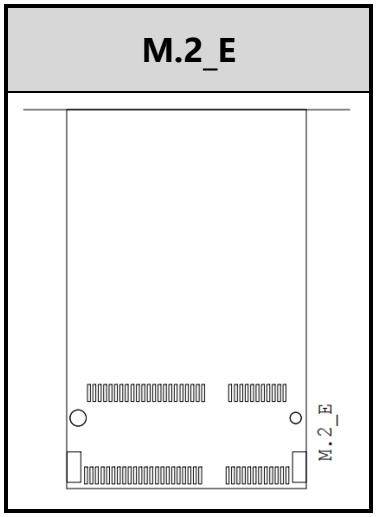
Pin	Signal
1	5V
2	GND
3	GND
4	12V

2.10 Expansion Slots (labeled as M.2_E, PCIEX4)

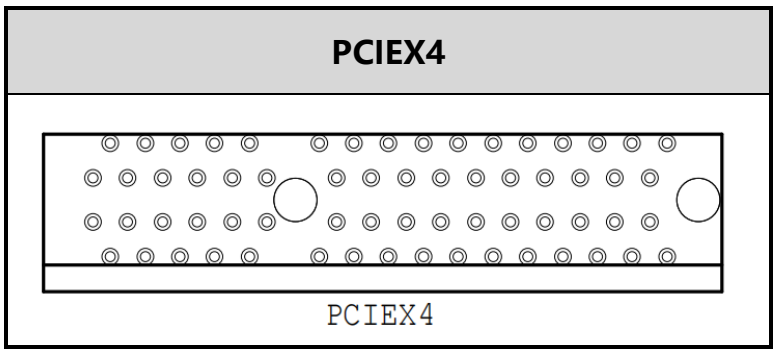
The board provides one M.2 Key E slot (labeled as M.2_E on the motherboard) for 2230 Wi-Fi and Bluetooth modules. The slot supports PCIe and USB 2.0 signals.

The board also features one PCIe x4 expansion slot (labeled as PCIEX4 on the motherboard) for PCIe expansion devices.

M.2_E: M.2 Key E slot



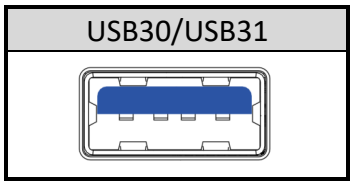
PCIE X4: PCIE X4 Slot



2.11 USB Interfaces (labeled as USB30, USB31, USB21, USB22)

USB 3.2

The board provides three USB 3.2 Gen 2 Type-A rear ports (labeled as USB30 and USB31 on the motherboard), supporting data transfer rates of up to 10 Gbps.



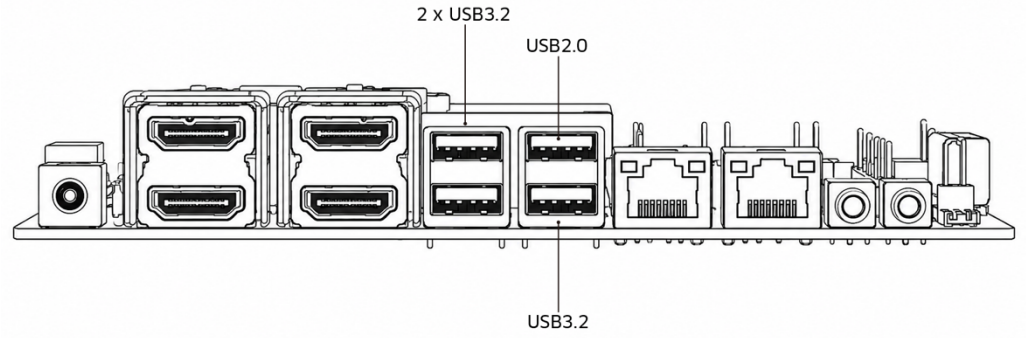
By default, the rear USB 3.2 Gen 2 Type-A ports (labeled as USB30 and USB31 on the motherboard) are powered by the 5V system rail. Optional 5V standby power is available upon request, enabling USB wake-up and power output of up to 5V/1A in system off or sleep states.

USB2.0

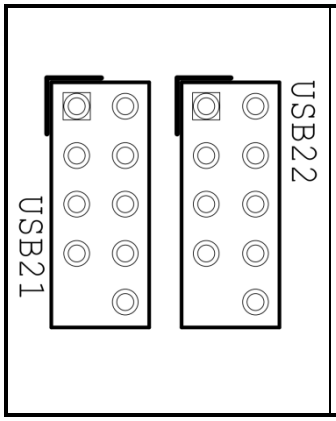
The board provides five USB 2.0 ports supporting data transfer rates of up to 480 Mbps, including

- 1 x USB 2.0 Type-A rear port (labeled as USB31 on the motherboard).
- 4 x USB 2.0 Type-A ports can be expanded through the USB21 and USB22 headers (2.54 mm pitch, labeled as USB21 and USB22 on the motherboard).
    - through the onboard CH334 USB hub controller and require driver installation.

The location of the USB interface is shown below.



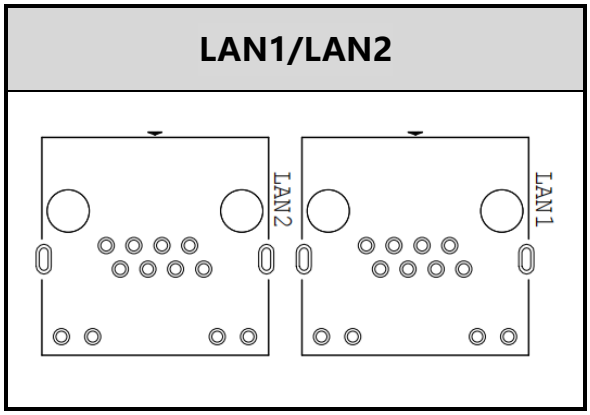
USB Header Pin Definition (labeled as USB21 / USB22):



Signal	Pin		Signal
VCC 5V	1	2	VCC 5V
USB DATA-	3	4	USB DATA-
USB DATA+	5	6	USB DATA+
GND	7	8	GND
NC	9	10	NC

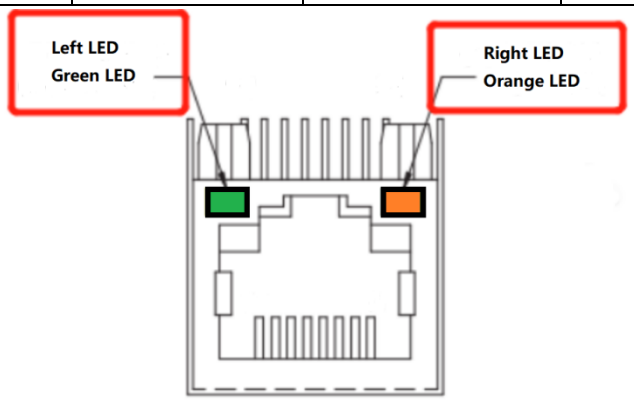
2.12 LAN (labeled as LAN1/LAN2)

The board provides two Gigabit Ethernet RJ45 ports powered by Realtek RTL8111H controllers. Both ports support Wake-on-LAN (WoL) via Magic Packet, while LAN1 additionally supports PXE boot.



LAN Port LED Status Indicators:

LI_LED (Green)	Function	ACT_LED (Orange)	Function
On	Link Established	Blinking	Network Activity



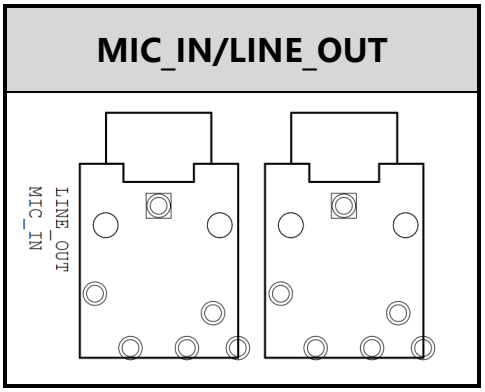
2.13 Audio Interfaces (labeled as FP_AUDIO and JAUD)

The board is equipped with the SenaryTech SN6186 high-definition audio codec.

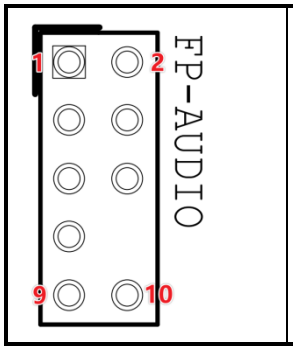
The rear I/O panel provides one set of 3.5 mm audio jacks (labeled as MIC_IN and LINE_OUT on the motherboard), including:

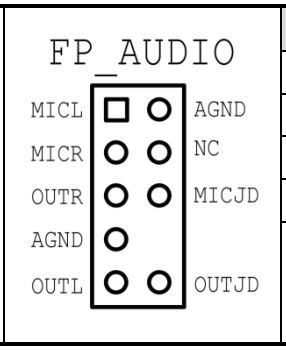
- LINE_OUT (Green): Audio output
- MIC_IN (Pink): Microphone input

The board also provides one front panel audio header, FP_AUDIO (2.54 mm pitch), and one amplifier output header, JAUD (2.0 mm pitch), labeled as FP_AUDIO and JAUD on the motherboard, respectively.



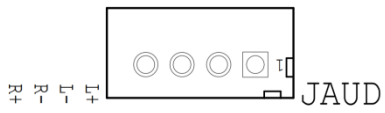
Front Panel Audio Header Pin Definition (labeled as FP_AUDIO, 2.54 mm pitch)





Signal	Pin		Signal
MIC2-L	1	2	AGND
MIC2-R	3	4	AVCC(NC)
FRO-R(OUTR)	5	6	MIC2-JD
F-IO-SEN(AGND)	7	8	NC
FRO-L(OUTL)	9	10	LIN2-JD

Amplifier Output Header Pin Definition (labeled as JAUD, 2.0 mm pitch)



Pin	Signal
1	L+
2	L-
3	R-
4	R+

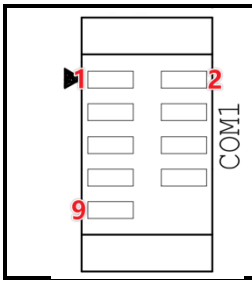
External Speaker Output Specifications (VDD = 5V)

Condition	Output Power
THD=1%, ClassD f=1KHz, RL=4Ω	2.1 W
THD=10%, ClassD f=1KHz, RL=4Ω	3.0 W
THD=1%, ClassD f=1KHz, RL=8Ω	1.4 W
THD=10%, ClassD f=1KHz, RL=8Ω	1.7 W

2.14 Serial Ports (Labeled as COM1/COM2/COM36)

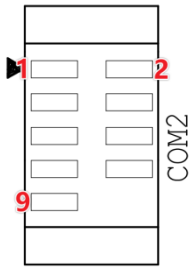
The board provides six serial ports through three onboard headers (2.0 mm pitch), labeled as COM1, COM2, and COM36 on the motherboard. All serial ports operate in RS-232 mode by default.
COM2 can be optionally configured to support RS-485 communication through hardware modification.

COM1 Header Pin Definition (labeled as COM1) (2.0mm)



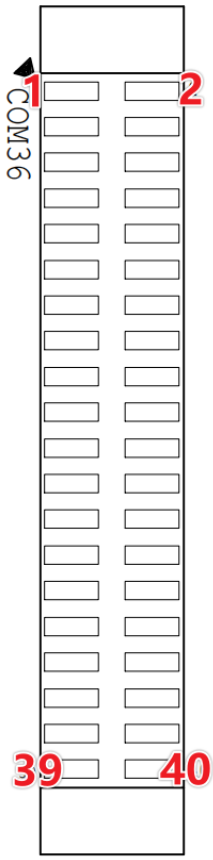
Signal	Pin		Signal
DCD#	1	2	DSR#
RXD	3	4	RTS#
TXD	5	6	CTS#
DTR#	7	8	RI#
GND	9		

COM2 Header Pin Definition (labeled as COM2) (2.0mm)



Pin	RS232	RS485(optional)
1	DCD#	DATA-
2	DSR#	DATA+
3	RXD	(NC)
4	RTS#	(NC)
5	TXD	(NC)
6	CTS#	(NC)
7	DTR#	(NC)
8	RI#	(NC)
9	GND	GND

COM36 Header Pin Definition (labeled as COM36) (2.0mm)



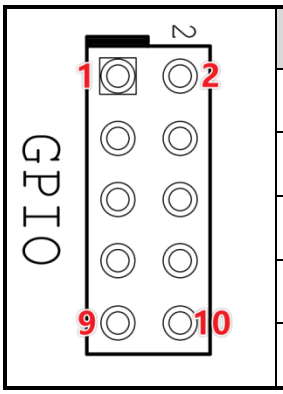
Signal	Pin		Signal
DCD#	1	2	RXD
TXD	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS#
RI#	9	10	(NC)
DCD#	11	12	RXD
TXD	13	14	DTR#
GND	15	16	DSR#
RTS#	17	18	CTS#
RI#	19	20	(NC)
DCD#	21	22	RXD
TXD	23	24	DTR#
GND	25	26	DSR#
RTS#	27	28	CTS#
RI#	29	30	(NC)
DCD#	31	32	RXD
TXD	33	34	DTR#
GND	35	36	DSR#
RTS#	37	38	CTS#
RI#	39	40	(NC)

2.15 GPIO (Labeled as GPIO)

The board provides one 2 × 5-pin GPIO header (2.0 mm pitch), labeled as GPIO on the motherboard. The header supports eight programmable general-purpose input/output (GPIO) signals.

GPIO settings are provided in the Appendix (GPIO_Setting).

GPIO(2.0mm)



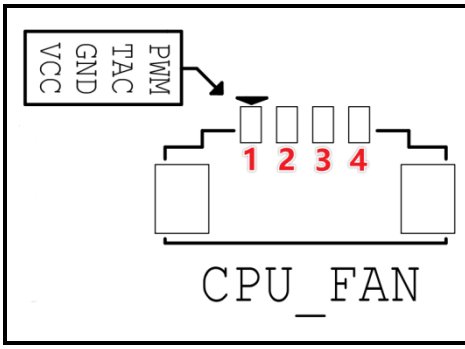
Signal	Pin		Signal
SIO_GP70	1	2	3.3V
SIO_GP71	3	4	SIO_GP74
SIO_GP72	5	6	SIO_GP75
SIO_GP73	7	8	SIO_GP76
GND	9	10	SIO_GP77

2.16 CPU Fan/System Fan Socket (Labeled as CPU_FAN, SYS_FAN)

The board provides the following fan interfaces:

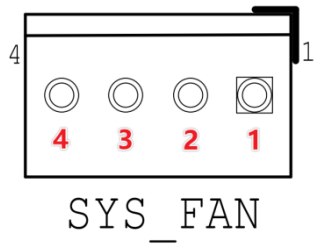
- **CPU_FAN:** One 4-pin CPU fan header (1.25 mm pitch), supporting 5V and 12V fans. A 5V CPU cooler is included by default.
- **SYS_FAN:** One 4-pin system fan header (2.54 mm pitch), supporting 5V and 12V fans.
- **JVCCFAN:** One fan voltage selection header (2.0 mm pitch) for selecting 5V or 12V fan operation.

CPU Fan Pin Definition (labeled as CPU_FAN)



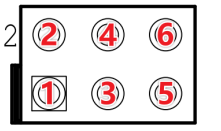
Pin	1	2	3	4
Signal	VCC	GND	TAC	CTL

System Fan Pin Definition (labeled as SYS_FAN)



Pin	4	3	2	1
Signal	CTL	TAC	VCC	GND

JVCCFAN Fan 5V/12V Voltage Adjustment Pins (labeled as JVCCFAN)

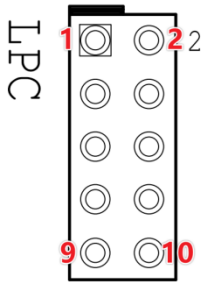


JVCCFAN		
	5V	12V
CPUFAN	1-3	3-5
SYSFAN	2-4	4-6

2.17 LPC Header (labeled as LPC)

The board provides one 2 × 5-pin LPC (Low Pin Count) header (2.0 mm pitch), labeled as LPC on the motherboard, for connecting external LPC devices.

LPC Header Pin Definition (labeled as LPC, 2.0 mm pitch)

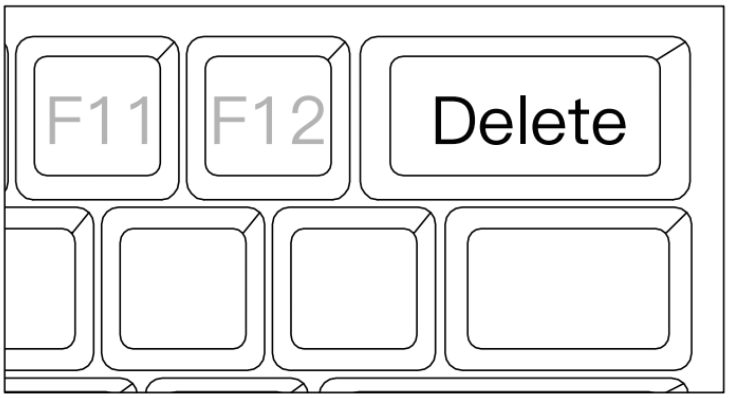


Signal	Pin		Signal
FRAME_N	1	2	LAD3
LAD2	3	4	LAD1
LAD0	5	6	GND
RLTRST_N	7	8	CLK
3.3V	9	10	SERIRQ

Chapter 3 BIOS Setup

3.1 Entering the BIOS

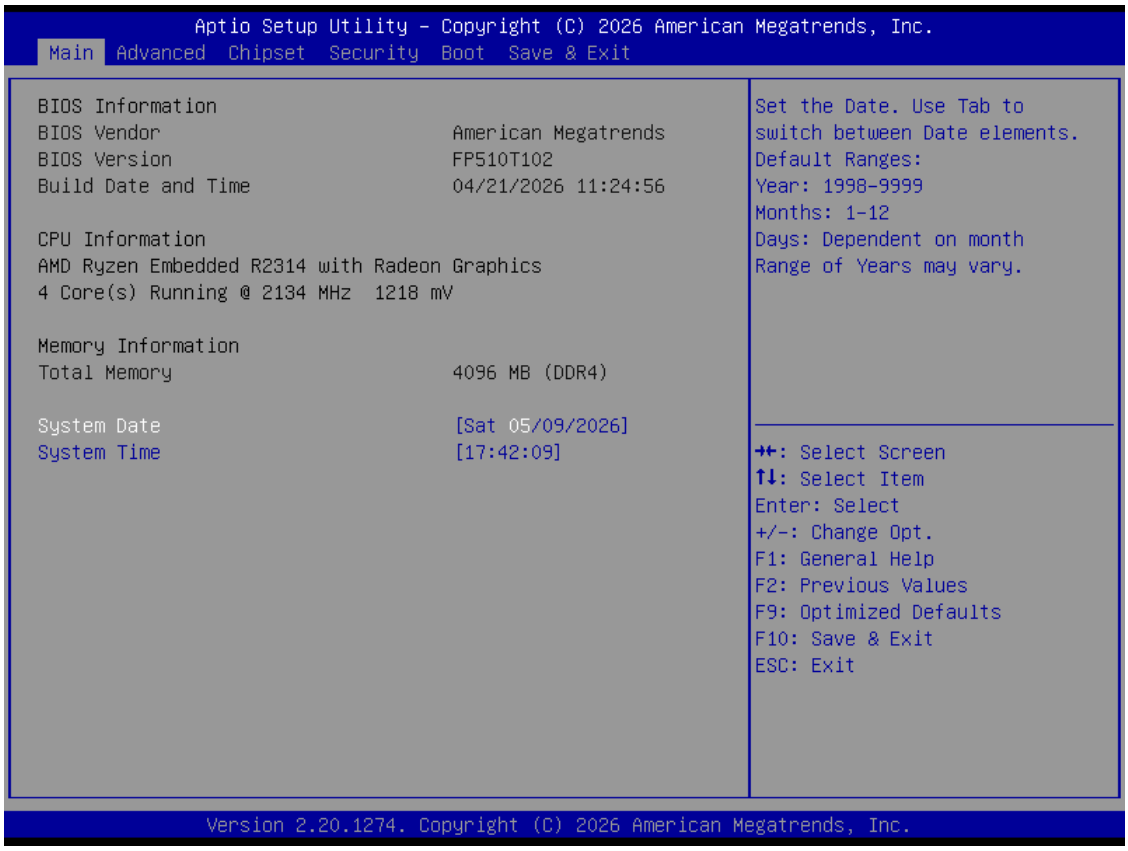
Entering BIOS Setup: Press the <Delete> key repeatedly during system startup to enter the BIOS Setup Utility.



BIOS Hot Keys:

Key	Function	Description
→ ←	Select Screen	Navigate between menu screens.
↑↓	Select Item	Move between menu items or options.
Enter	Select	Open a submenu or confirm a selection.
+/-	Change Option	Adjust values or change settings.
F1	General Help	Displays helpful information for the selected item.
F2	Previous Values	Load the previously saved settings.
F9	Optimized Defaults	Restore factory default settings.
F10	Save & Exit	Save changes and exit BIOS.
ESC	Exit	Exit BIOS or return to the previous menu.

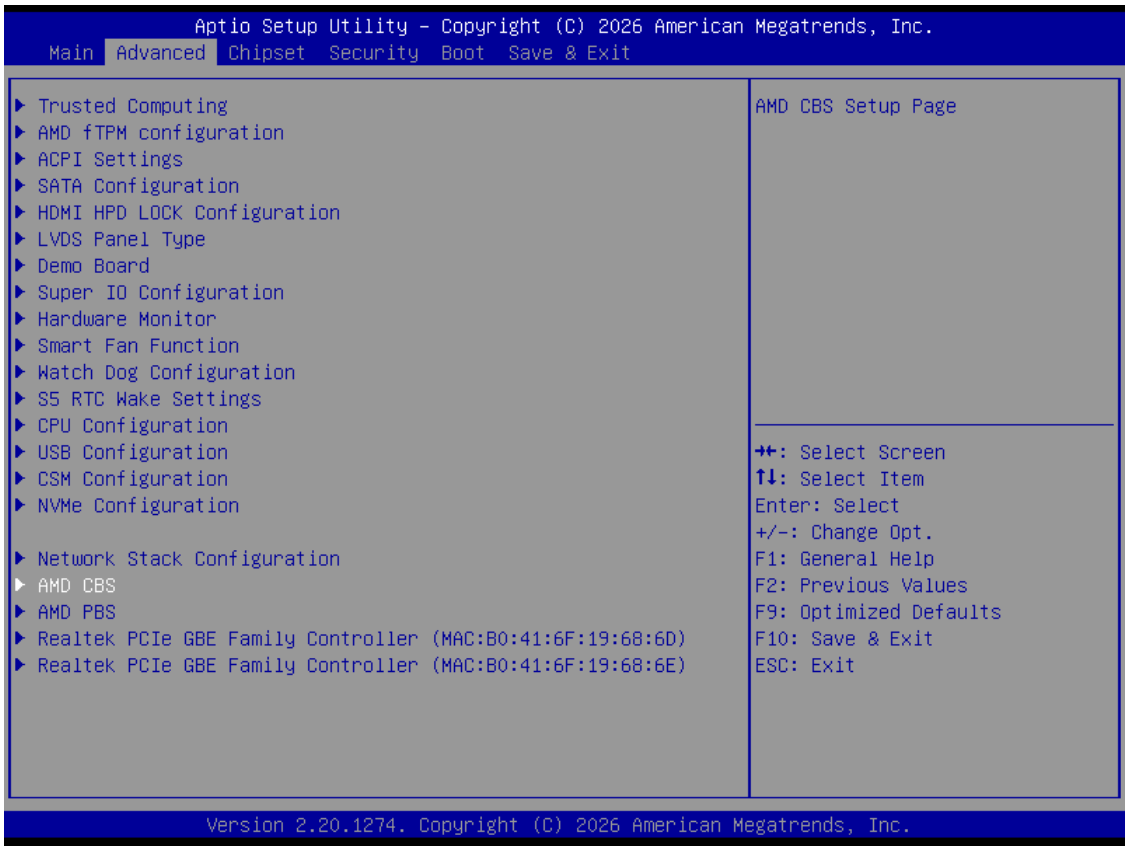
3.2 Main Menu (BIOS Info, Date, Time)



BIOS Information

- BIOS Vendor: American Megatrends
- BIOS Version: Displays the current BIOS version
- Build Date and Time: BIOS build timestamp
- Processor Information: CPU identification details
- Total Memory: Installed system memory
- Memory Frequency: Active memory operating frequency
- PCH Information: Platform Controller Hub details
- PCH SKU: PCH model identifier
- ME FW Version: Intel Management Engine firmware version
- System Date: System date setting (format: MM/DD/YYYY)
- System Time: System time setting (format: HH:MM:SS)

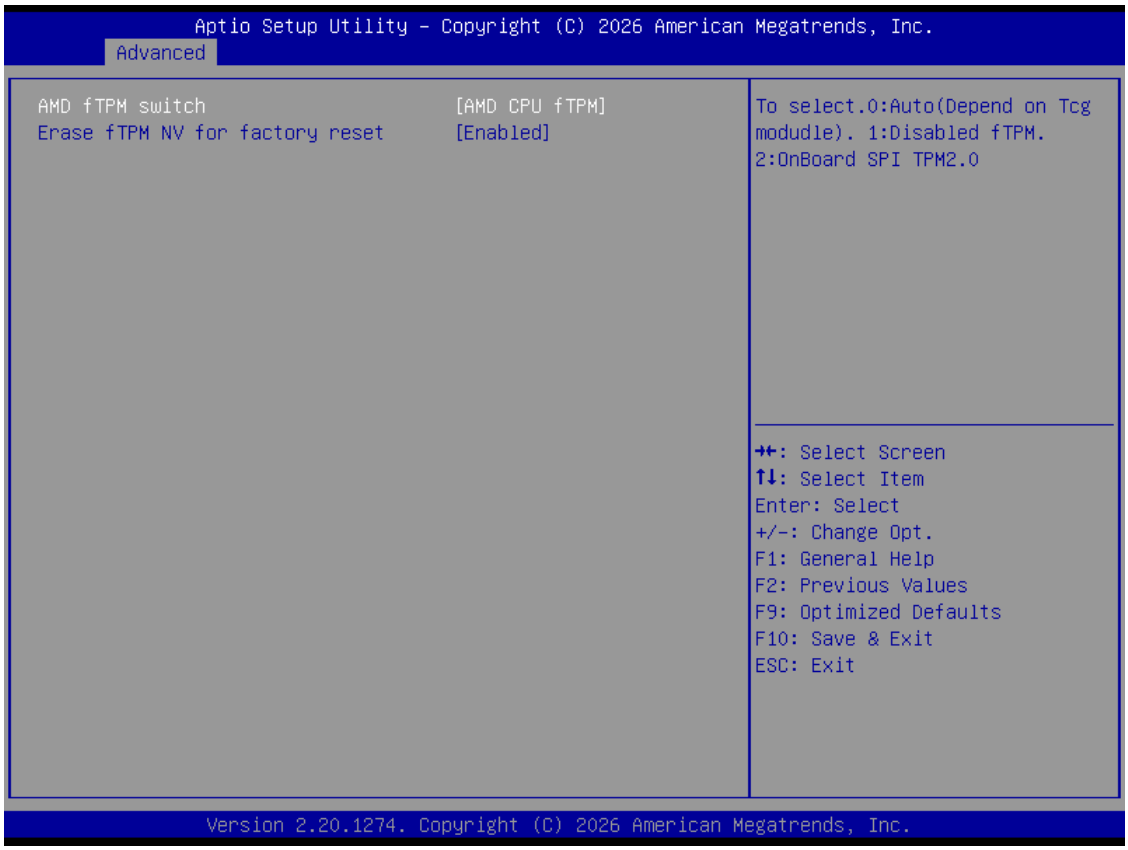
3.3 Advanced Settings



Selecting any item in the left pane opens its corresponding Advanced submenu. The Advanced section allows you to configure system features, adjust platform behavior, and modify CPU-related settings. The available submenus include:

- Trusted Computing
- AMD fTPM Configuration
- ACPI Settings
- SATA Configuration
- HDMI HPD Lock Configuration
- LVDS Panel Type
- Demo Board (Not Supported)
- Super I/O Configuration
- Hardware Monitor
- Smart Fan Function
- Watchdog Configuration
- S5 RTC Wake Settings
- CPU Configuration
- USB Configuration
- CSM Configuration
- NVMe Configuration (Not Supported)

3.3.1 AMD fTPM configuration



AMD fTPM Configuration

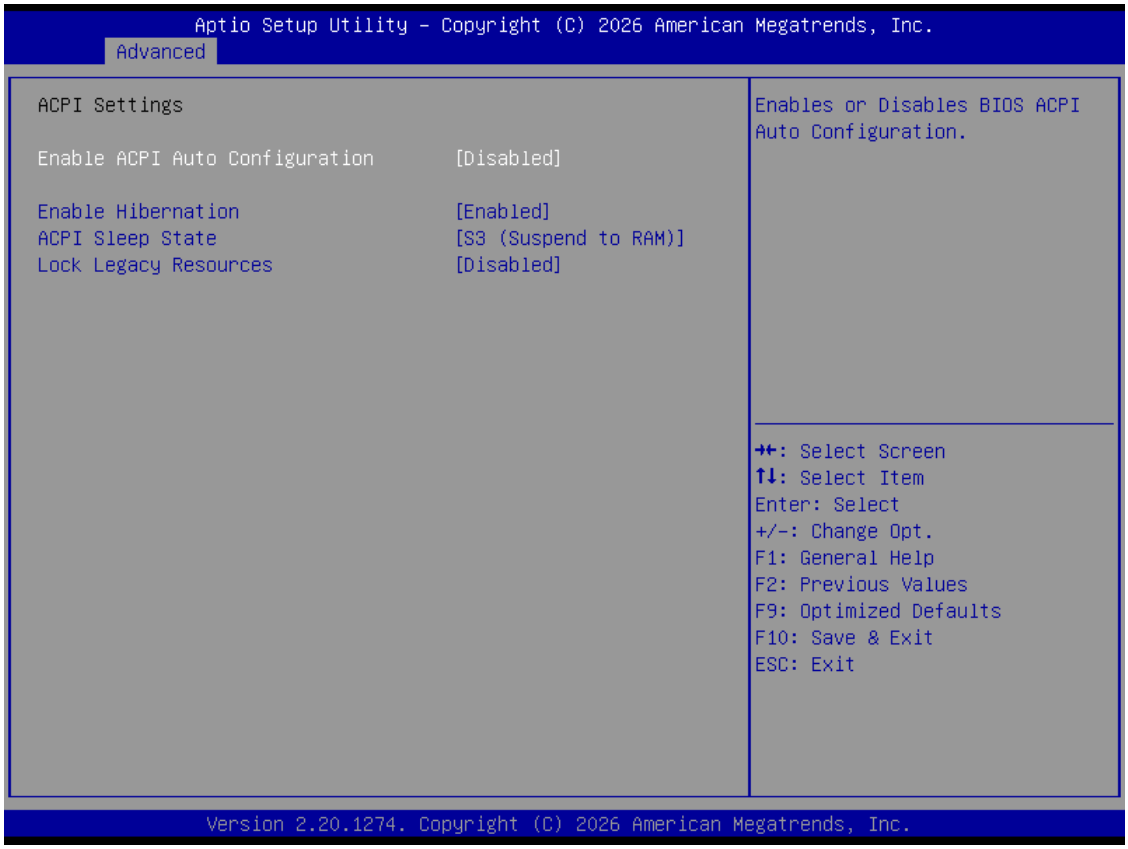
AMD fTPM Switch: Select the TPM device used by the system.

- AMD CPU fTPM: Uses the processor's integrated firmware TPM.
- Route to LPC TPM: Uses an external TPM module via the LPC interface. An optional External TPM module is required.

Erase fTPM NV for Factory Reset

- Enable or disable fTPM reset for newly installed CPUs.
- Default: Enabled

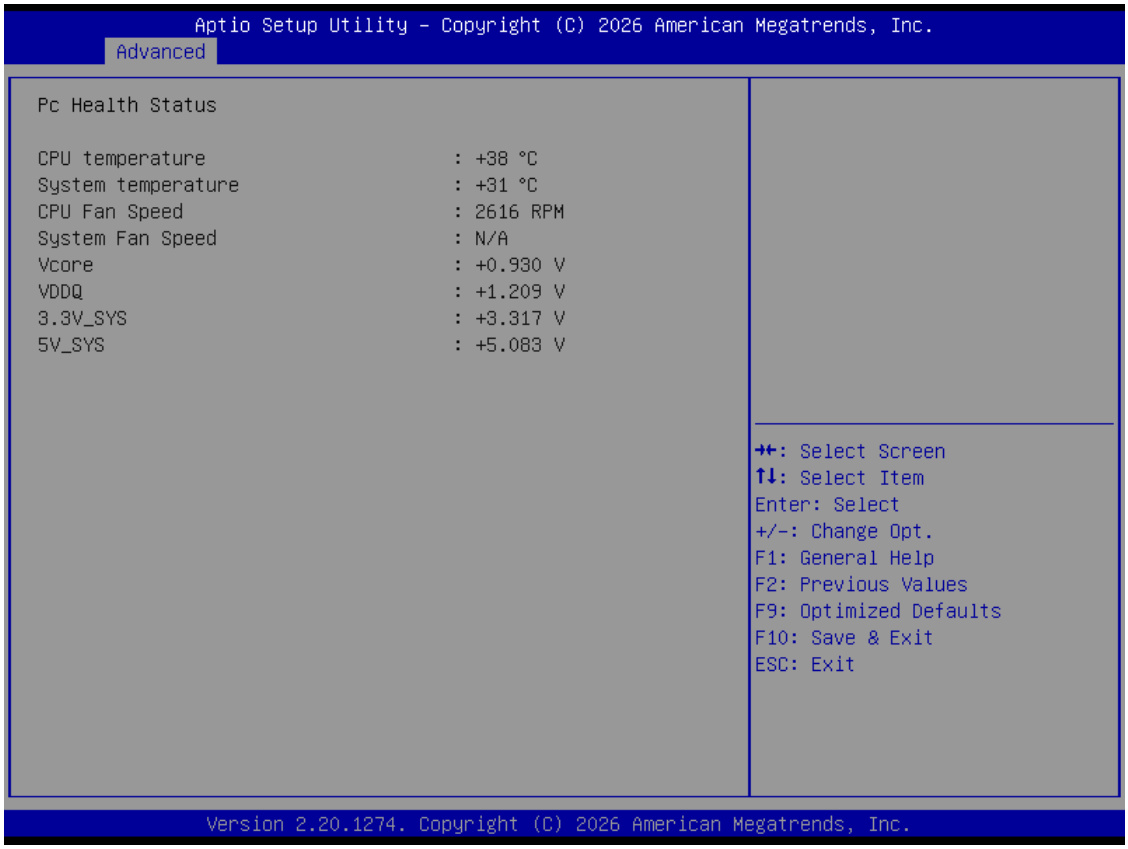
3.3.2 ACPI Settings



ACPI Settings

- **Enable ACPI Auto Configuration**: Enables or disables automatic ACPI configuration. Disabled by default.
- **Enable Hibernation**: Enables or disables system hibernation support.
- **ACPI Sleep State**: Selects the system ACPI sleep state.
- **Lock Legacy Resources**: Enables or disables locking of legacy system resource

3.3.3 Hardware Monitor

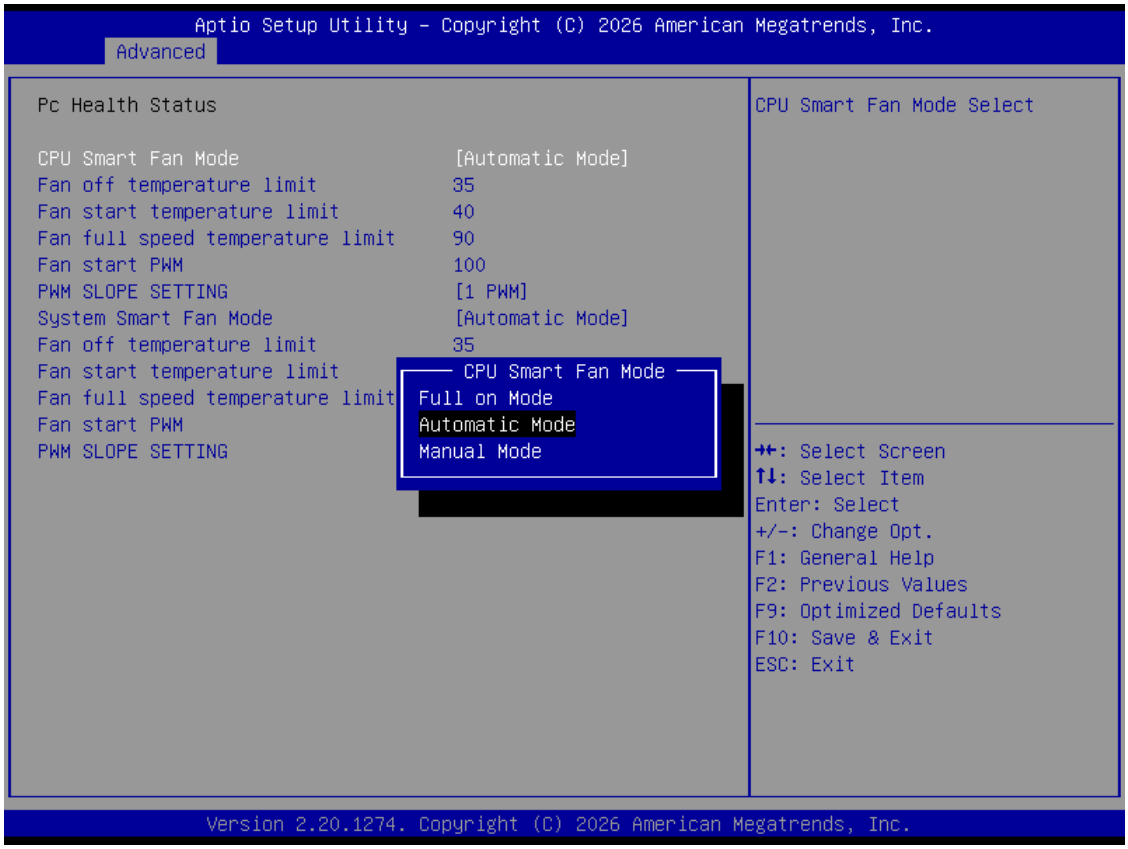


PC Health Status

The PC health status displays CPU temperature, system temperature, fan speed, and other relevant voltage values.

- **CPU Temperature:** Displays the current CPU temperature.
- **System Temperature:** Displays the current system temperature.
- **CPU Fan Speed:** Displays the current CPU fan speed.
- **System Fan Speed:** Displays the current system fan speed.
- **Vcore:** Displays the CPU core voltage.
- **VDDQ:** Displays the memory I/O voltage.
- **3.3V_SYS:** Displays the system 3.3 V voltage.
- **5V_SYS:** Displays the system 5 V voltage

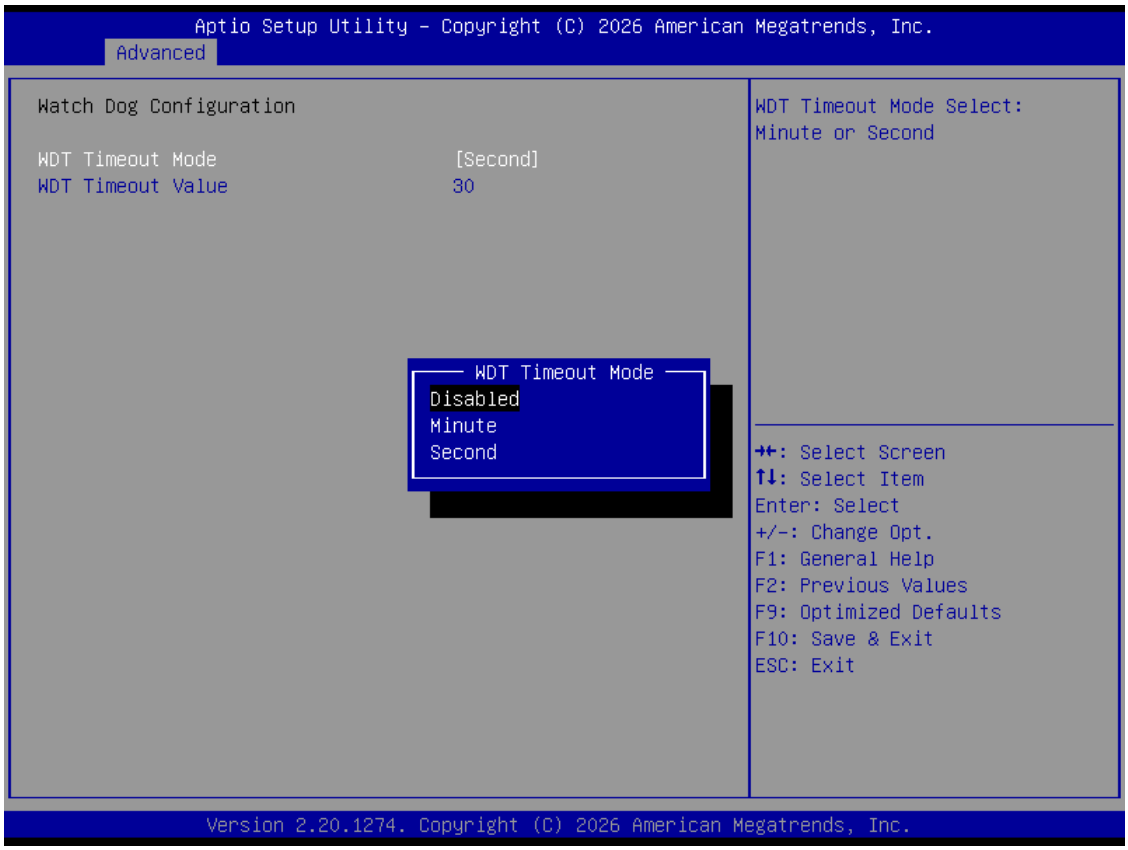
3.3.4 Smart Fan Function



PC Health Status → Smart CPU_Fan Mode

- **Smart CPU_Fan Mode / Smart SYS_Fan Mode:** Enables or disables smart fan control for the CPU fan or system fan.
- **Automatic Mode:** Automatically adjusts fan speed based on system temperature. (Default mode)
- **Full On Mode:** Forces the fan to operate at full speed continuously.
- **Manual Mode:** Allows manual configuration of fan speed control parameters.
- **Fan Off Temperature Limit:** the temperature threshold below which the fan stops.
- **Fan Start Temperature Limit:** the temperature at which the fan starts operating.
- **Fan Full Speed Temperature Limit:** the temperature at which the fan runs at full speed.
- **Fan Start PWM:** the initial PWM duty cycle when the fan starts.
- **PWM Slope Setting:** Adjusts the rate at which PWM duty cycle increases with temperature.

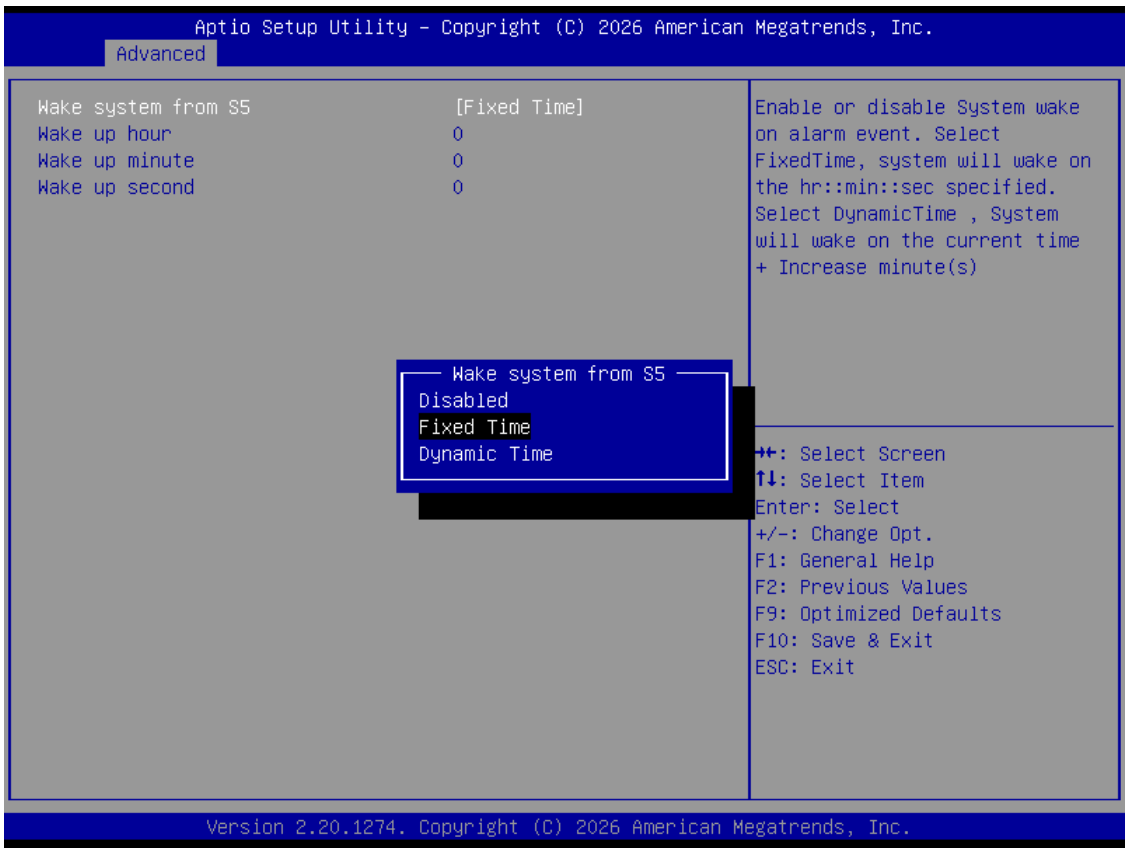
3.3.5 Watch Dog Configuration



Watch Dog Configuration

- WDT Timeout Mode: Select Minute or Second

3.3.6 S5 RTC Wake Settings



S5 RTC Wake Settings

- **Wake System From S5**: Enables or disables automatic system power-on from the S5 (shutdown) state.

  Default: Disabled

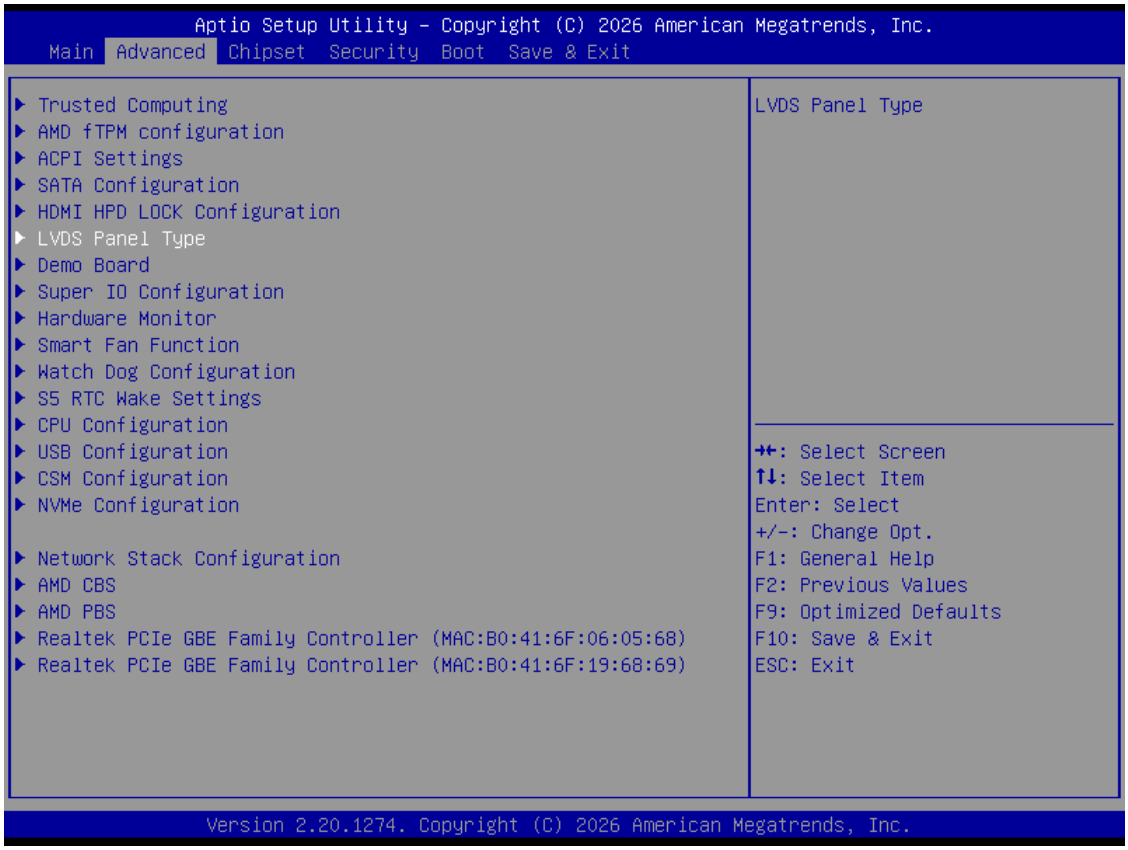
- **Wake Time Mode**: Selects the wake-up timing mode.
  - **Fixed Time**: When selected, the system wakes at the specified **Hour : Minute : Second**.
  - **Dynamic Time**: When selected, the system wakes after a dynamically calculated time interval.

3.3.7 LVDS Panel Type

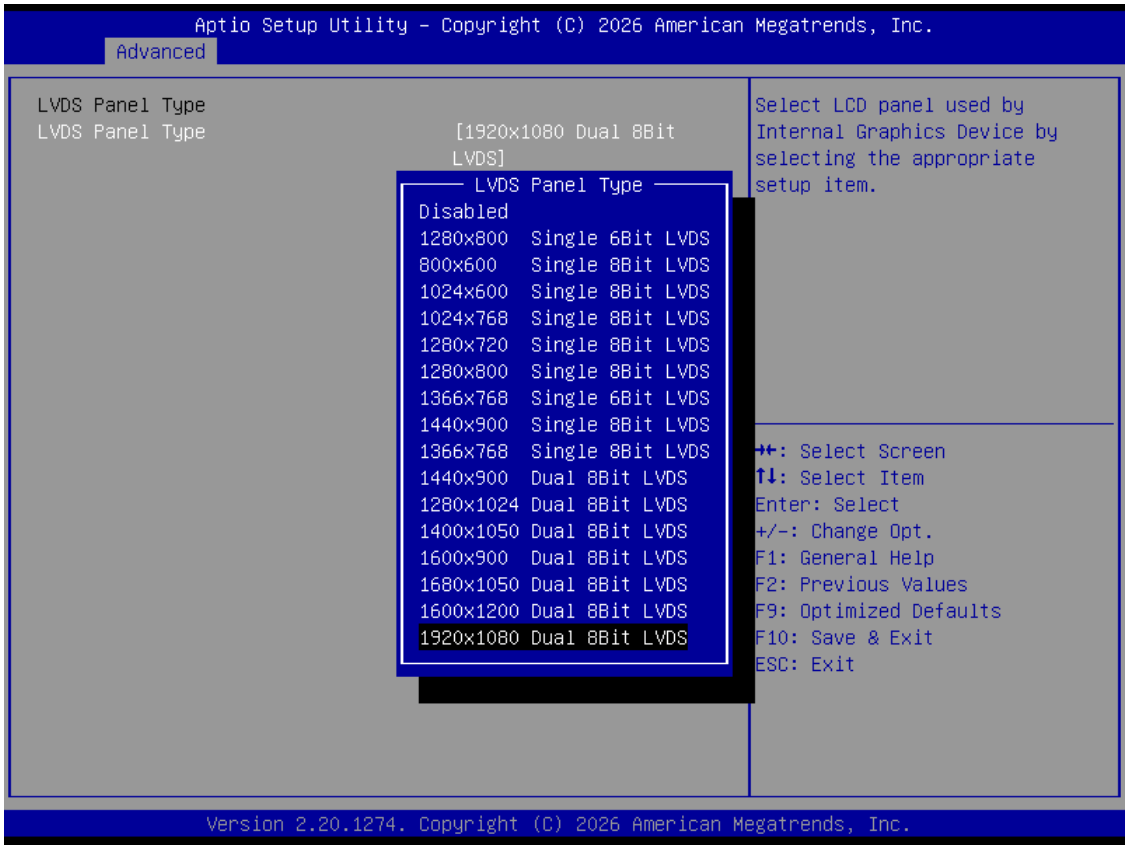
This section describes how to enable LVDS output and configure LCD panel parameters.

Configuration Steps:

1. Power on the system and press Delete to enter the BIOS Setup Utility. Navigate to Advanced → LVDS Panel Type, then press Enter.



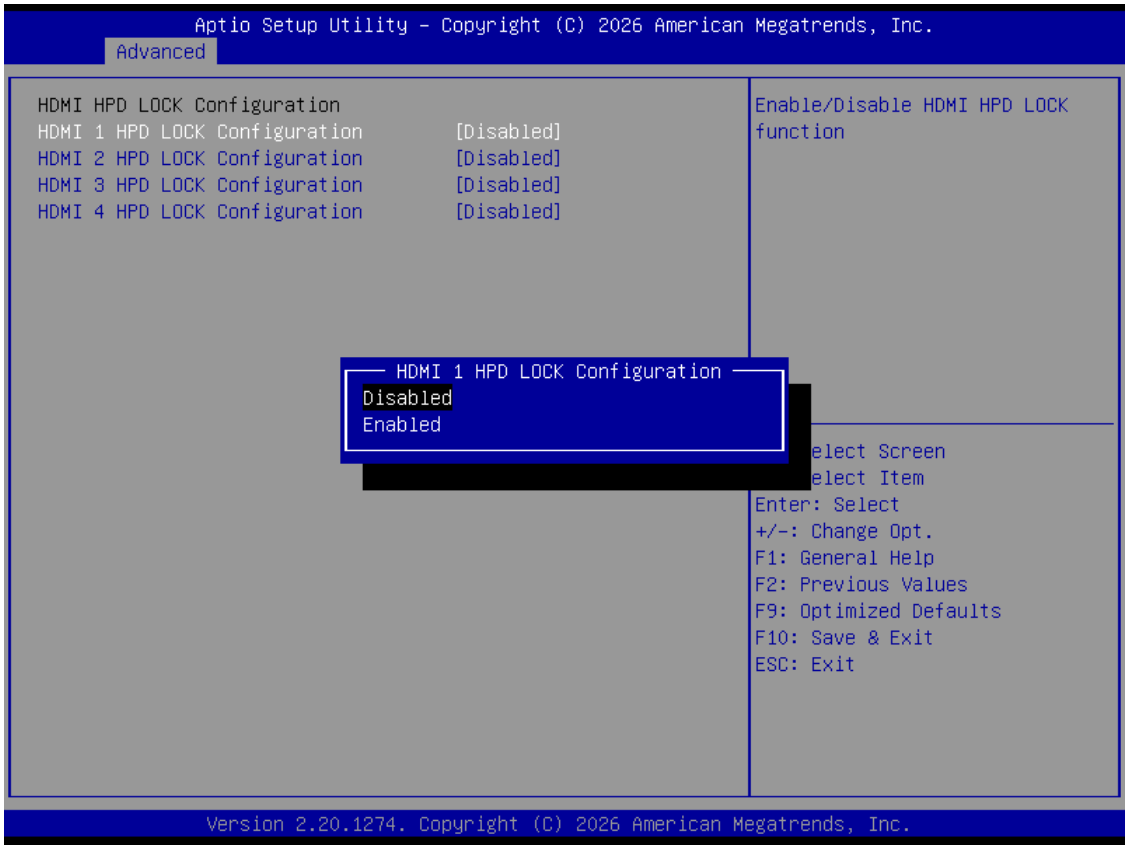
2. Select **LCD Panel Type**.
   - The default setting is **Disabled**, which turns off LVDS output.
   - Select the required LVDS resolution to enable LVDS. Panel parameter options correspond to the LCD panel specifications (such as resolution, color depth, and channel configuration). Configure the setting according to the panel's specification sheet.



Note

- By default, LVDS/eDP output is disabled.
- Once LVDS or eDP is enabled, the LVDS/eDP interface becomes the primary display output. All BIOS setup screens will be displayed only on the LVDS/eDP panel.
- Other display outputs (such as HDMI) will not display the BIOS interface while LVDS/eDP is active.
- Ensure that the LCD panel parameters are configured correctly before connecting the LVDS display.
- If incorrect panel parameters are selected and no display is shown, restore default settings by clearing the CMOS, then reconfigure the LVDS panel settings.

3.3.8 HDMI HPD LOCK Configuration



Configure HDMI Hot Plug Detect (HPD) lock settings for each HDMI port.

HDMI 1 HPD Lock Configuration

- Enable or disable HDMI HPD lock for HDMI 1. When enabled, the display output remains active even if the connected display is disconnected or powered off.

HDMI 2 HPD Lock Configuration

- Enable or disable HDMI HPD lock for HDMI 2.

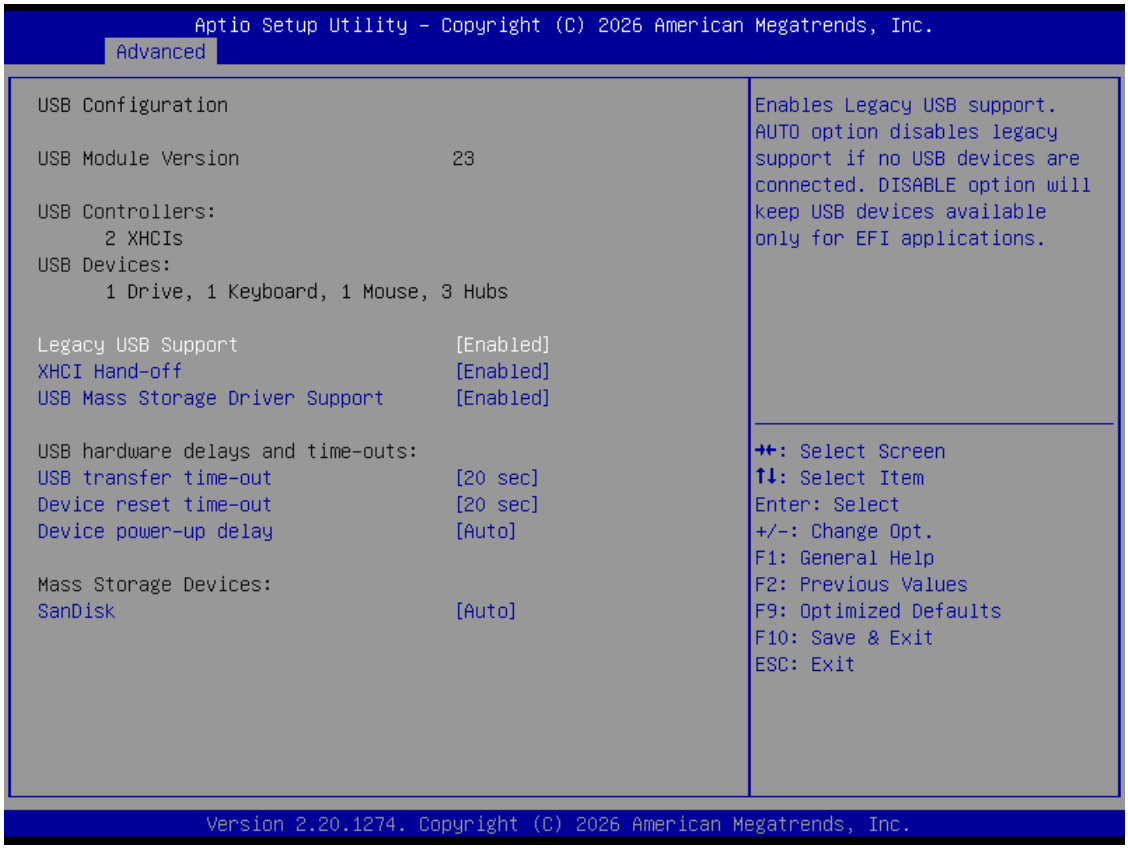
HDMI 3 HPD Lock Configuration

- Enable or disable HDMI HPD lock for HDMI 3.

HDMI 4 HPD Lock Configuration

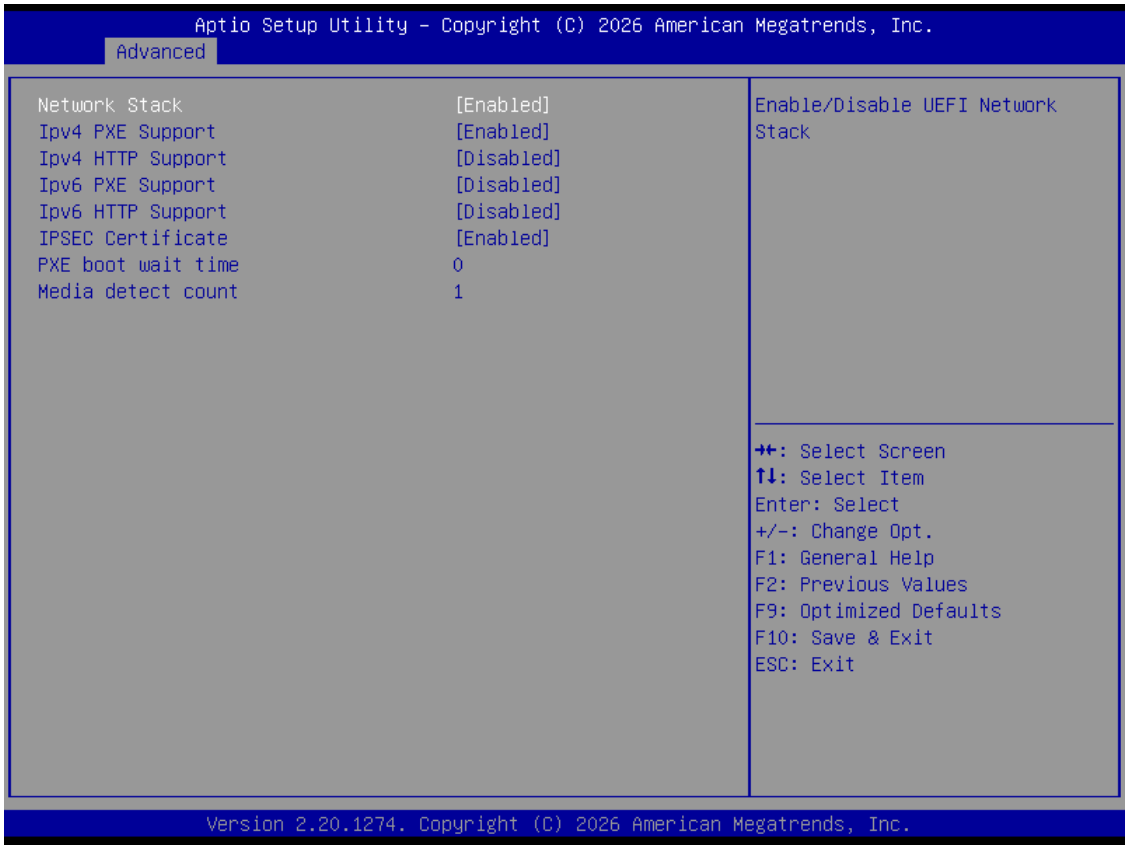
- Enable or disable HDMI HPD lock for HDMI 4.

3.3.9 USB Configuration



- **Legacy USB Support:** Enable Legacy USB support. Disables legacy support if no USB devices are connected. Select enable will keep USB devices available under UEFI's support.
- **XHCI Hand-off:** A workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the USB XCHI driver.
- **USB Mass Storage Driver Support:** Enable(default) or disable USB Mass Storage Driver Support.
- **USB transfer time-out:** Time-out value for control, bulk, and interrupt transfers, default time:20 second.
- **Device reset time-out:** USB mass storage device starts unit command time-out, default time:20 second.
- **Device Power-up Delay:** Maximum time the device will take before it properly reports itself to the host controller.

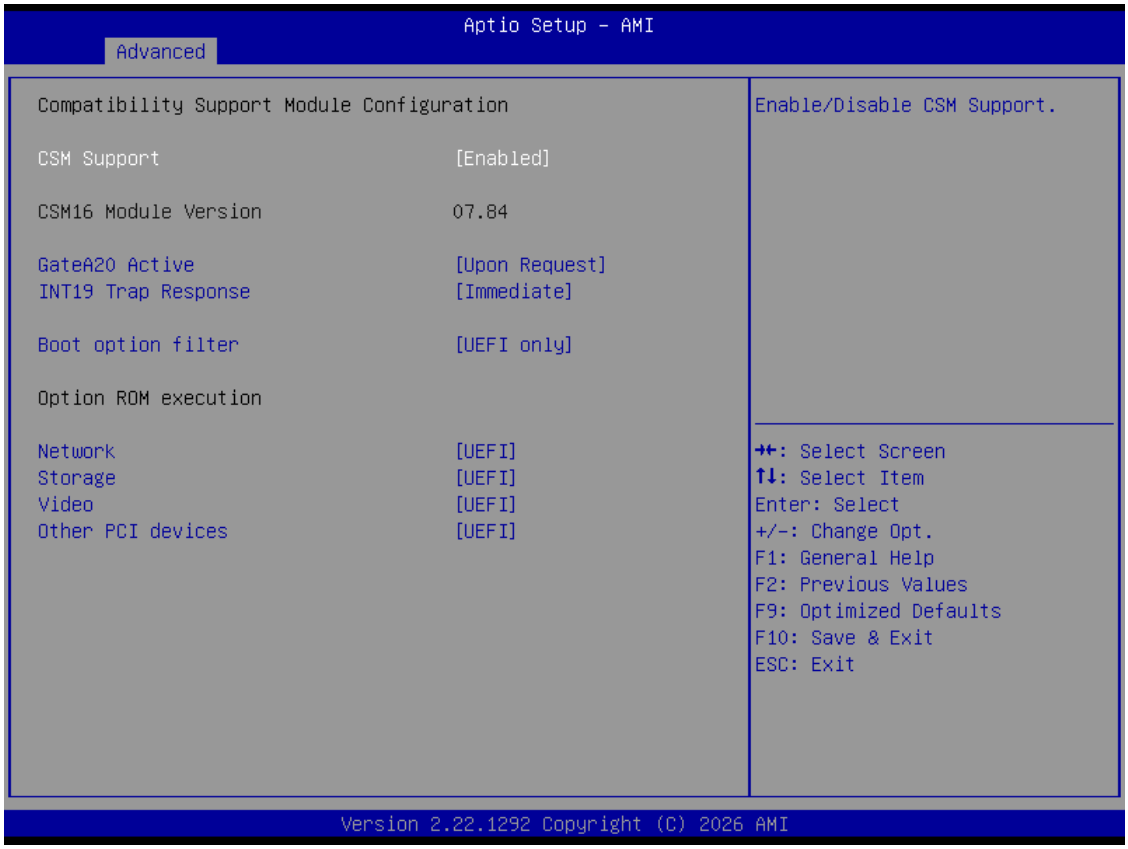
3.3.10 Network Stack Configuration



The Network Stack controls UEFI network boot (PXE/HTTP) and is disabled by default.

- **IPv4 PXE Support:** PXE boot over IPv4
- **IPv4 HTTP Support:** HTTP boot over IPv4
- **IPv6 PXE Support:** PXE boot over IPv6
- **IPv6 HTTP Support:** HTTP boot over IPv6
- **PXE Boot Wait Time:** Timeout delay for PXE boot
- **Media Detect Count:** Retry count for network device detection

3.3.11 CSM Support



CSM Support: Configure the Compatibility Support Module (CSM) for operating systems that do not support UEFI boot. **Enabled (Default):** Enables CSM support. **Disabled:** Disables CSM support**.**

Note: CSM remains enabled when the system is configured to boot in Legacy mode.

Boot Option Filter: Select the supported boot mode.

- **UEFI Only:** Supports UEFI boot only.
- **Legacy Only:** Supports Legacy BIOS boot only.
- **UEFI and Legacy:** Supports both UEFI and Legacy BIOS boot.

Option ROM Execution: Configure the execution mode of Option ROMs for different device types.

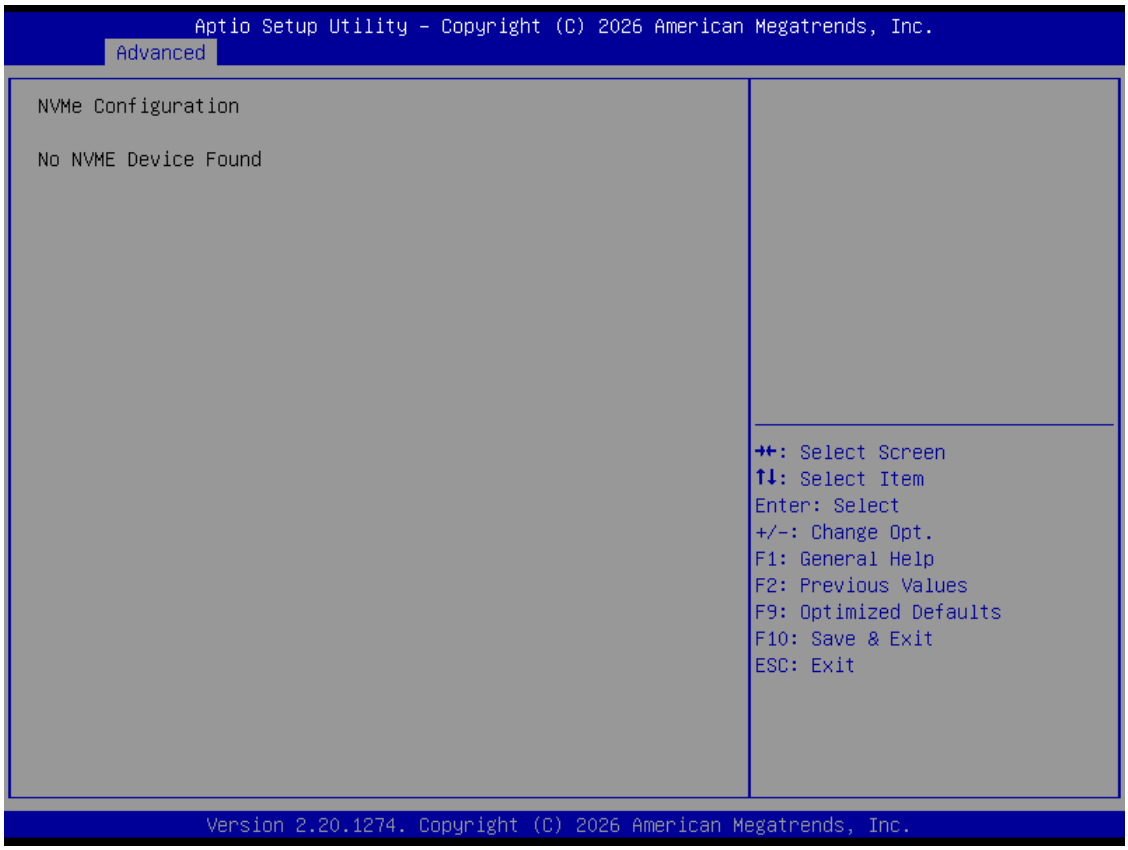
Available settings:

- **Do Not Launch:** Does not load the device Option ROM.
- **UEFI:** Loads the device Option ROM in UEFI boot mode.
- **Legacy:** Loads the device Option ROM in Legacy boot mode.

The following device categories can be configured independently:

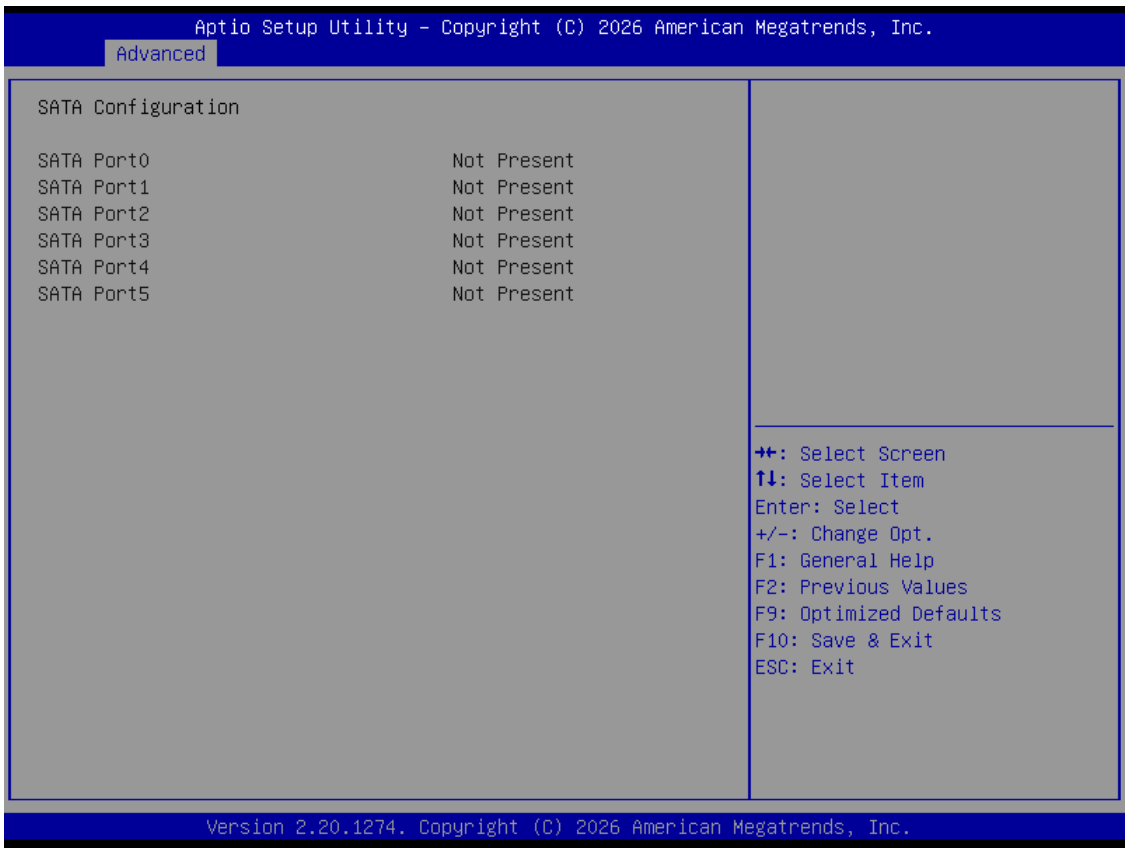
- **Network:** Configure the Option ROM execution mode for network devices.
- **Storage:** Configure the Option ROM execution mode for storage devices.
- **Video:** Configure the Option ROM execution mode for display devices.
- **Other PCI Devices:** Configure the Option ROM execution mode for other PCI devices.

3.3.12 NVME Configuration



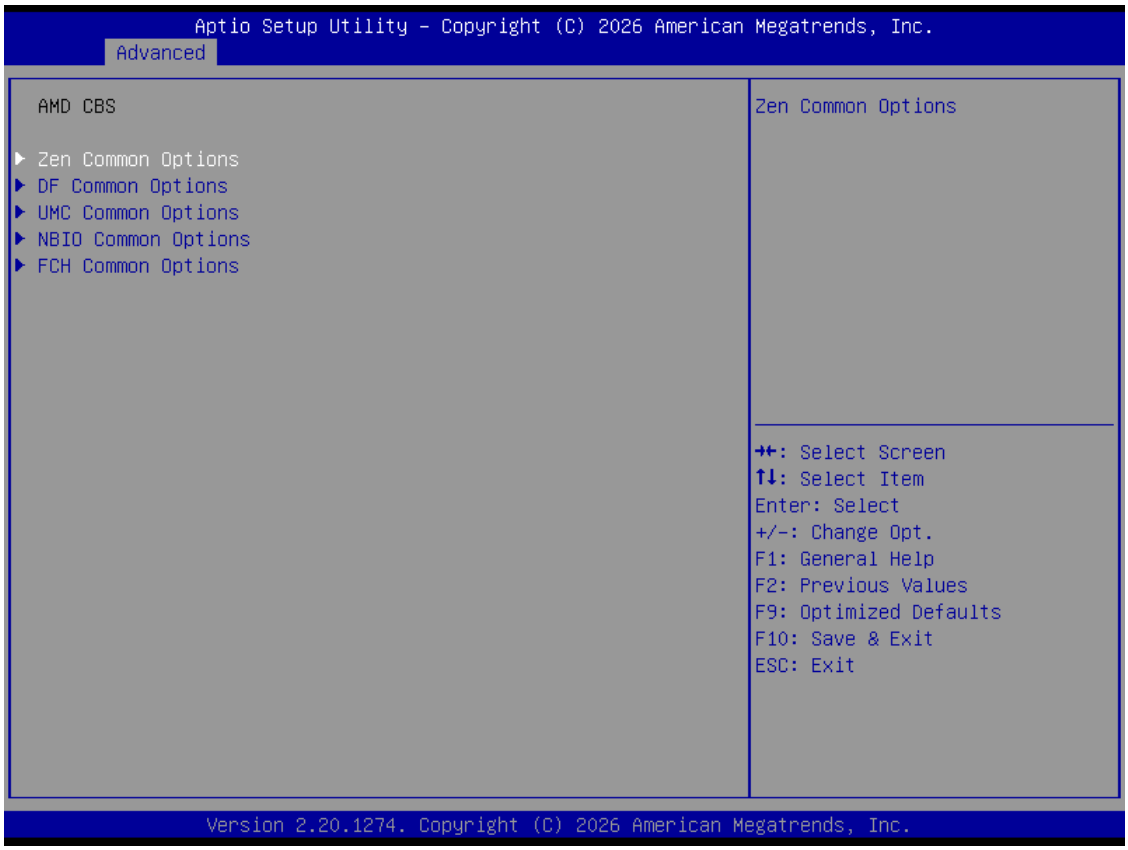
When an NVMe SSD is installed, this menu displays information such as the drive model and storage capacity.

3.3.13 SATA Configuration



When a SATA storage device is installed, this menu displays information such as the drive model and storage capacity.

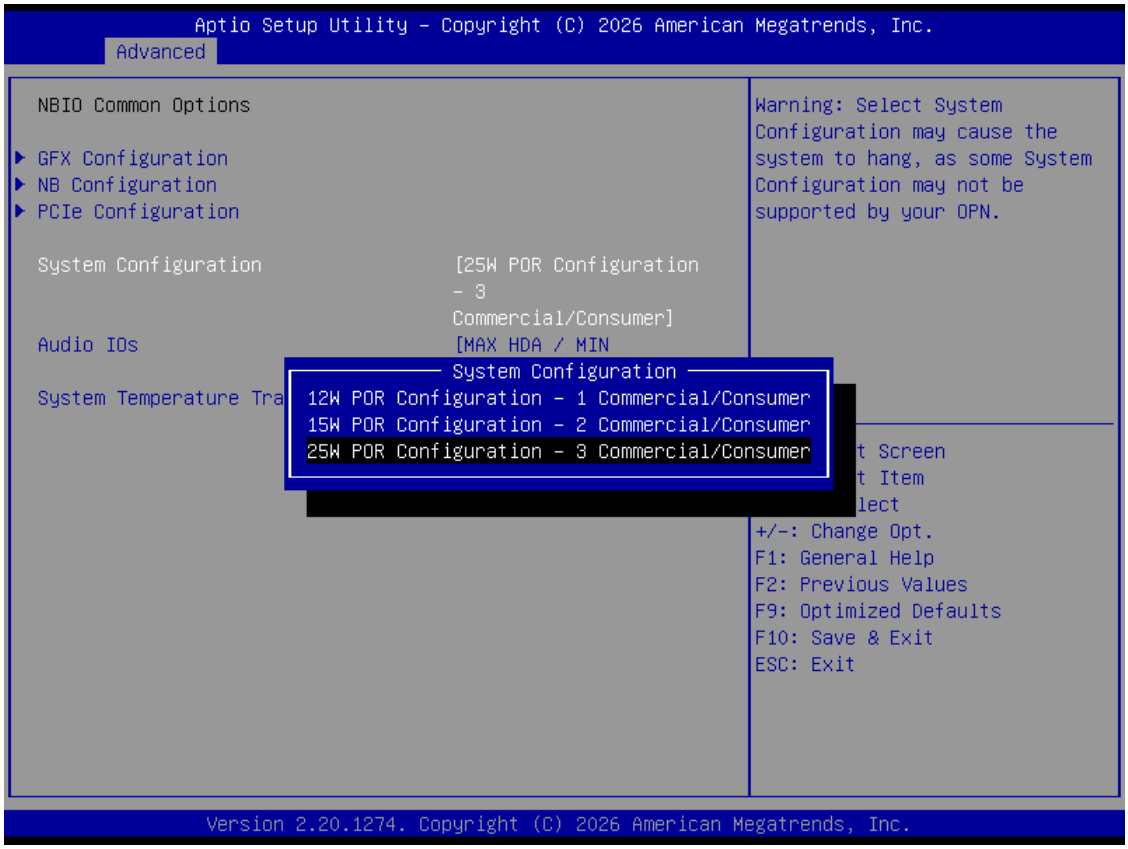
3.3.14 AMD CBS



The AMD CBS (Common BIOS Settings) menu provides access to advanced AMD platform configuration options.

- **Zen Common Options:** CPU configuration options
- **DF Common Options:** Data Fabric configuration options
- **UMC Common Options**: Unified Memory Controller options
- **NBIO Common Options:** Northbridge I/O options
- **FCH Common Options:** Fusion Controller Hub options

3.3.15 NBIO Common Options



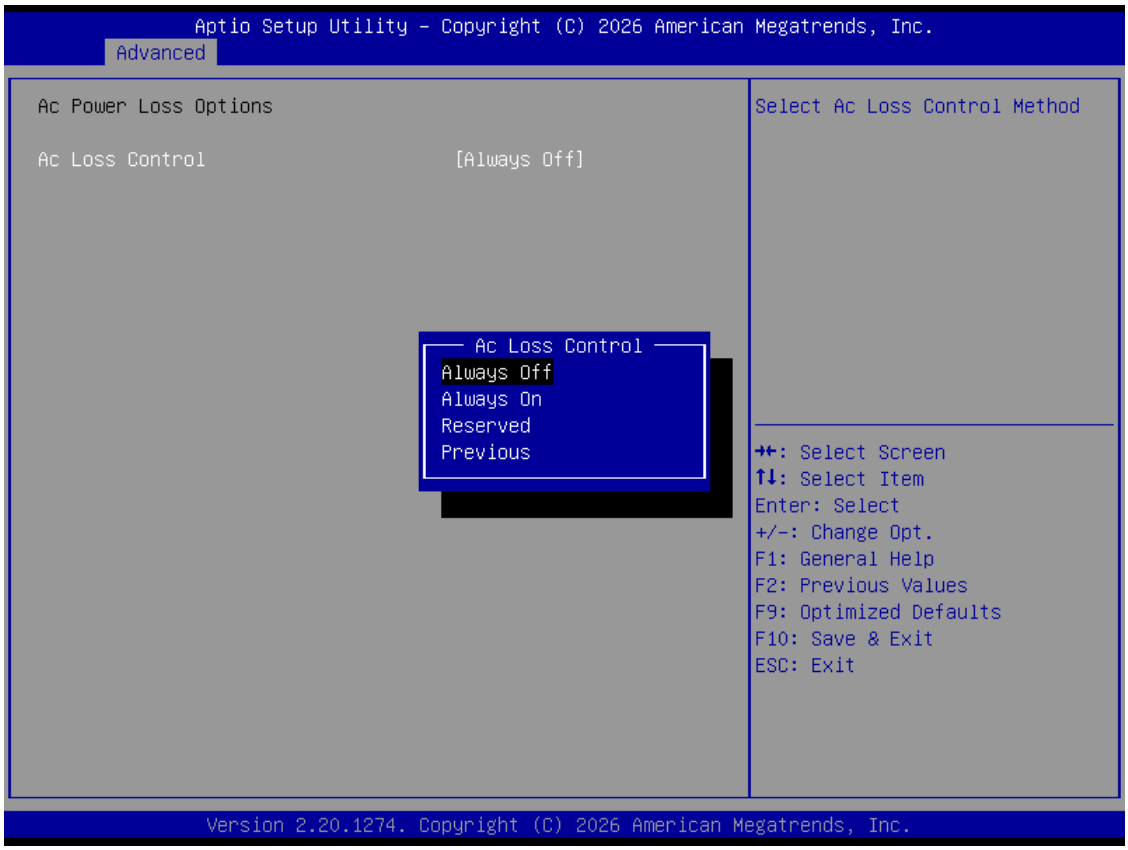
NBIO Common Options

System Configuration: This menu allows users to configure the CPU TDP limit according to system cooling capabilities.

- **12W:** Low power consumption
- **15W (Default):** Balanced performance and power consumption
- **25W:** Maximum performance (requires adequate cooling)

Advanced → AMD CBS → NBIO Common Options → System Configuration → 12W/15W/25W POR Configuration → 1/2/3 Commercial/Consumer

3.3.16 FCH Common Options



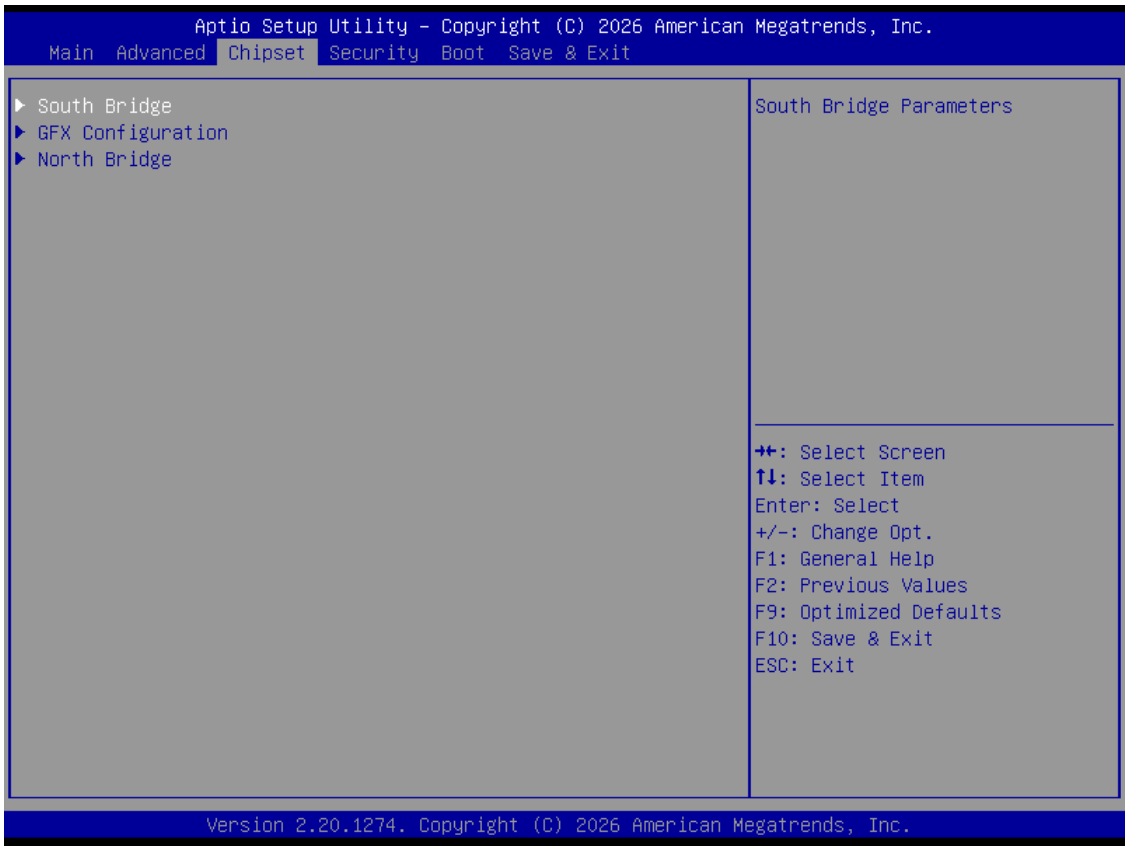
The FCH Common Options configure chipset-level power management and ACPI-related behavior, including system power-on behavior after AC power restoration.

Advanced > AMD CBS > FCH Common Options > AC Loss Control

AC Power Loss Options: Controls system behavior after AC power is restored.

- **Always Off (Default):** The system remains powered off when AC power is restored.
- **Always On:** The system automatically powers on when AC power is restored.
- **Reserved/Previous:** The system remains off after a normal shutdown. If AC power is lost unexpectedly, the system restores its previous power state when power is recovered**.**

3.4 Chipset

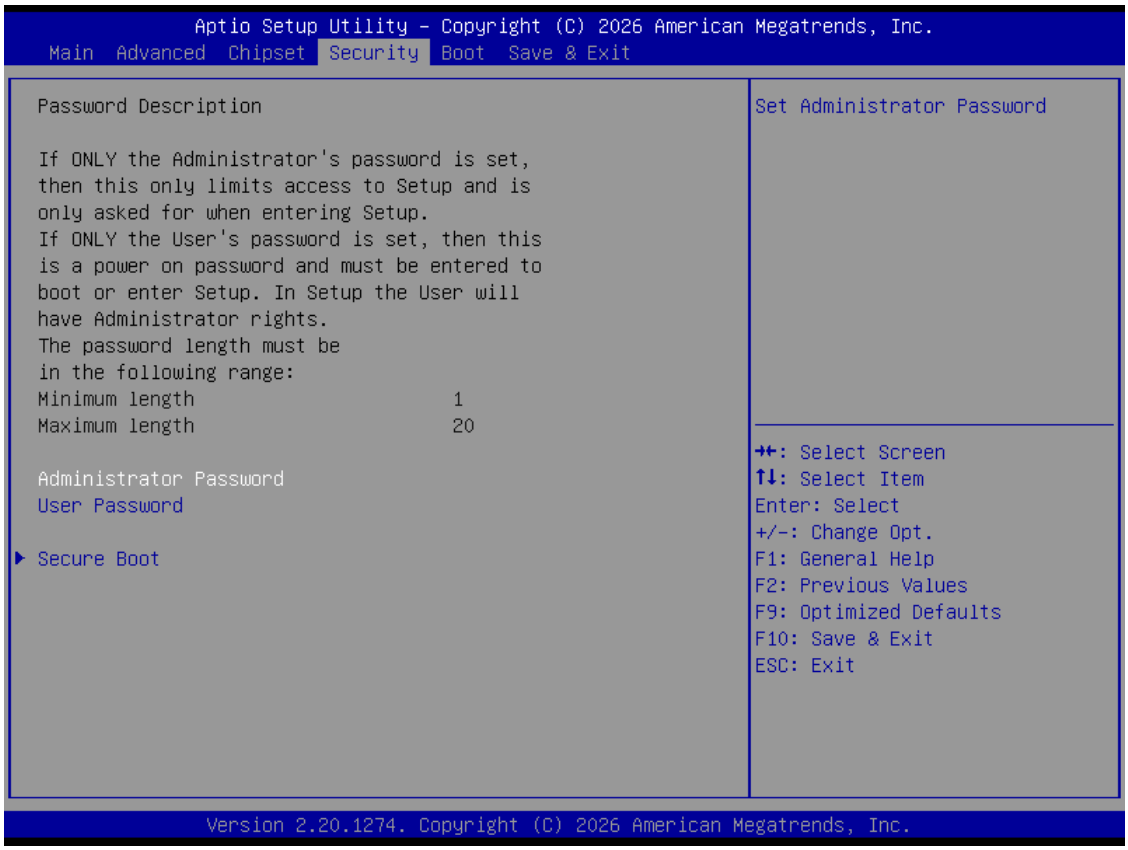


South Bridge: Configures South Bridge–related settings and peripheral functions.

GFX Configuration (Not Supported): Configures integrated graphics settings.

North Bridge: Configures North Bridge–related settings.

3.5 Security

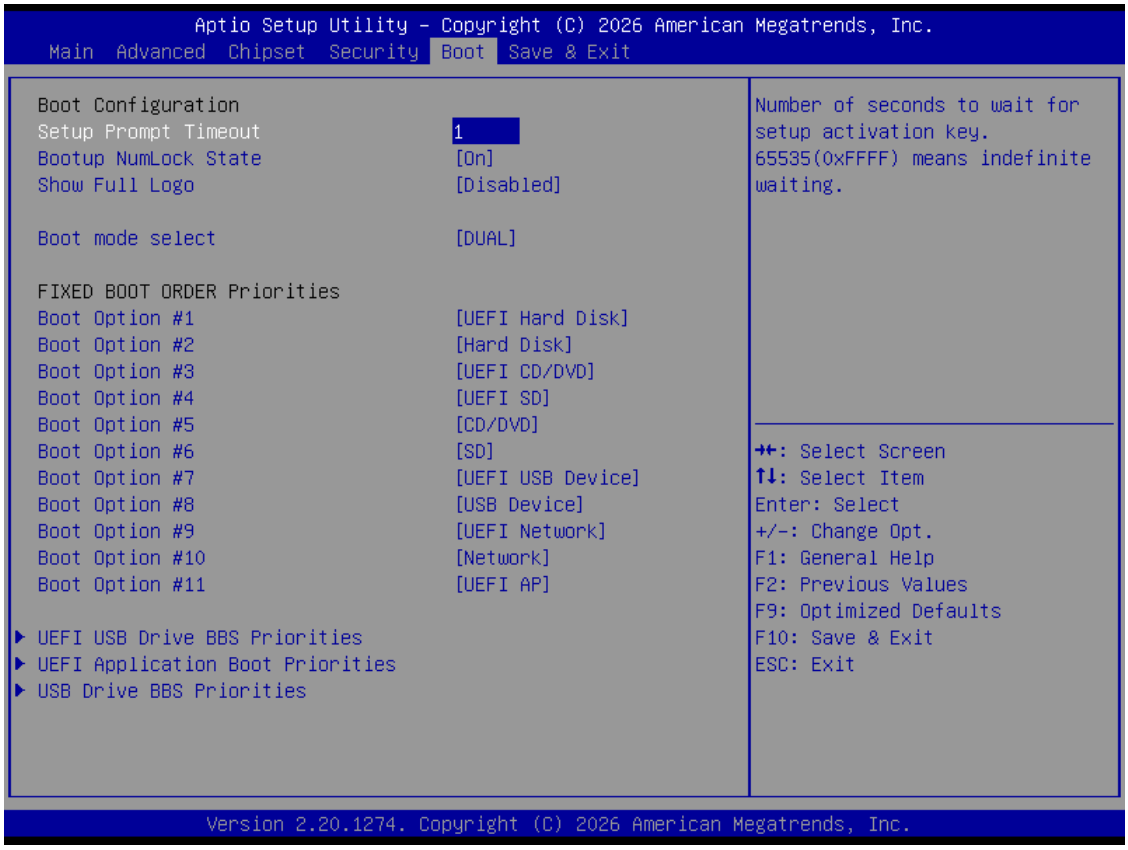


Administrator Password: Set the Administrator Password.

User Password: Set User Password.

Secure Boot: Configures Secure Boot settings.

3.6 BOOT



Boot Configuration

Setup Prompt Timeout: Sets the timeout period before the default boot option is initiated. A value of **0** starts the default boot option immediately, while **65535 (0xFFFF)** causes the firmware to wait indefinitely for user input before booting.

Bootup NumLock State: Selects the keyboard NumLock state after system startup.

- **On (Default):** Enables the numeric keypad for number entry.
- **Off:** Configures the numeric keypad to operate as cursor control keys.

Show Full Logo: Enables or disables the display of the customized boot logo.

- **Enabled:** Displays the boot logo.
- **Disabled:** Hides the boot logo.

Boot Mode Select: Selects the system boot mode.

- **UEFI:** Supports UEFI boot only.
- **Legacy:** Supports Legacy BIOS boot only.
- **Dual (Default):** Supports both UEFI and Legacy BIOS boot.

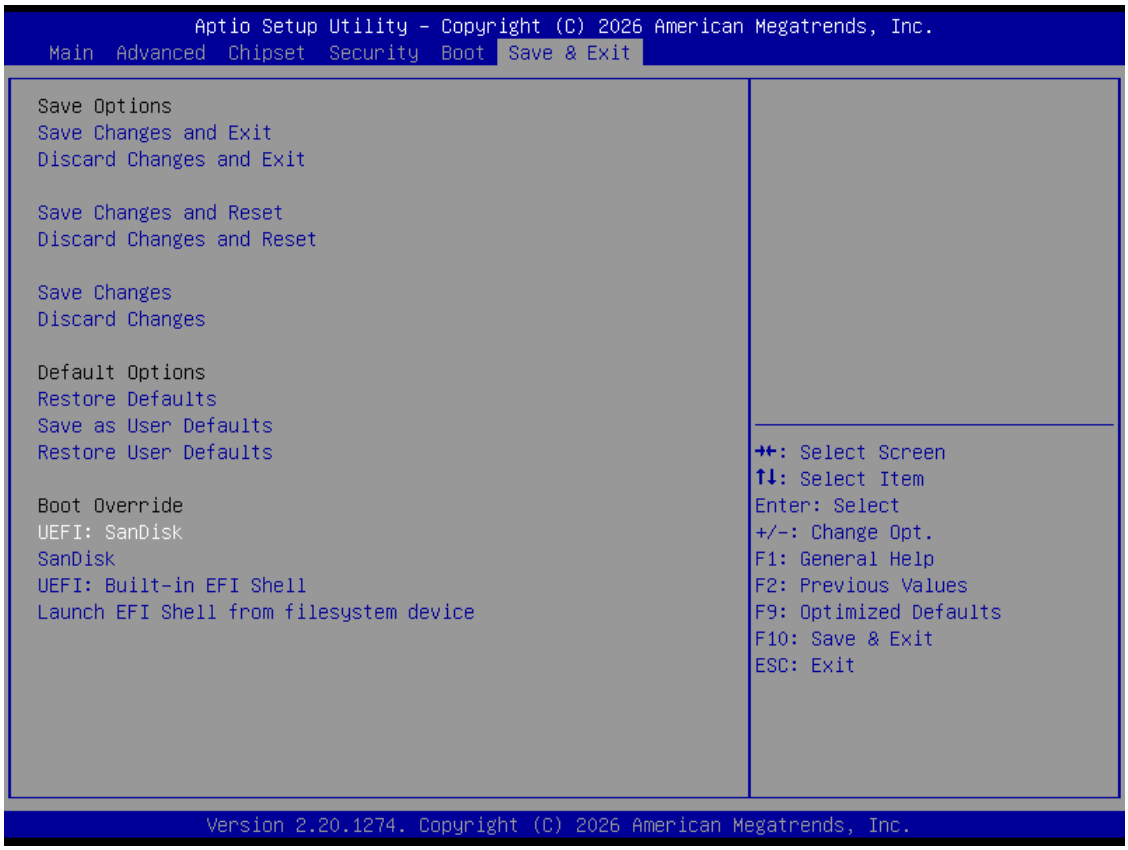
Boot Option #1–#11: Configures the boot priority order of available boot devices.

UEFI USB Drive BBS Priorities: Configures the boot priority of UEFI USB storage devices.

UEFI Application Boot Priorities: Configures the boot priority of UEFI applications.

USB Drive BBS Priorities: Configures the boot priority of USB storage devices.

3.7 Save & Exit



Save Changes and Exit: Exit the system setup after saving the changes and continue to start the computer.

Discard Changes and Exit: Exit the system setup without saving any changes and continue to start the computer.

Save Changes and Reset: Reset the system after saving the changes.

Discard changes and Reset: Reset the system without saving any changes.

Save Changes: Save changes done so far to any of the options.

Discard Changes: Discard changes done so far to any of the options.

Restore Defaults: Restore/load default values for all the options.

Save as User Defaults: Save the changes done so far as the user defaults.

Restore User Defaults: Restore the user defaults to all the options.

Boot Override: Boot device selection can override your boot priority. Select the specified boot device such as SATA, USB Flash Disk, EFI Shell, PXE, etc., and boot directly. Or press F11 boot by selecting the specified boot device.

- **UEFI: Built-in EFI Shell**: Launches the built-in UEFI EFI Shell.
- **Launch EFI Shell From Filesystem Device**: Launches the EFI Shell from a filesystem device.

Appendix

GPIO Setting

Accessing GPIO70:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x01); //Bit0=1 set as output，bit0=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x01); // When set as output, Bit0 of I/O address 0xA06 = 1 outputs high level, Bit0 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit0=1 Set as output，bit0=0 Set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); //When set as input, Bit0 of I/O address 0xA06 reflects the read state.

Accessing GPIO71:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x02); // Bit1=1 set as output， bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x02); // When set as output, Bit1 of I/O address 0xA06 = 1 outputs high level, Bit1 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); // Bit0=1 set as output， bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit1 of I/O address 0xA06 reflects the read state.

Accessing GPIO72:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x04); //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x04); // When set as output, Bit2 of I/O address 0xA06 = 1 outputs high level, Bit2 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit2 of I/O address 0xA06 reflects the read state.

Accessing GPIO73:

Example: Accessing via IO

Set as output：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x08); //Bit3=1 set as output，bit3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x08); // When set as output, Bit3 of I/O address 0xA06 = 1 outputs high level, Bit3 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit3=1 set as output，bi3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit3 of I/O address 0xA06 reflects the read state.

Accessing GPIO74:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x10); //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x10); // When set as output, Bit4 of I/O address 0xA06 = 1 outputs high level, Bit4 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit4 of I/O address 0xA06 reflects the read state.

Accessing GPIO75:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x20);    //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x20); // When set as output, Bit5 of I/O address 0xA06 = 1 outputs high level, Bit5 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit5 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO76:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x40); //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x40); // When set as output, Bit6 of I/O address 0xA06 = 1 outputs high level, Bit6 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit6 of I/O address 0xA06 reflects the read state.

Accessing GPIO77:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x80); //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x80); // When set as output, Bit7 of I/O address 0xA06 = 1 outputs high level, Bit7 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit7 of I/O address 0xA06 reflects the read state.