# User Manual

AL-35



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# Warning

1. Before using the product, carefully read the manual to ensure proper installation and operation.
2. If you are not ready to install any extension card, store it in an anti-static protective bag to prevent damage.
3. To discharge any static electricity, briefly touch a grounded metal object before removing the extension card from the protective bag.
4. Always wear anti-static gloves and handle the card by its edges to avoid damaging sensitive components.
5. Verify that the power supply voltage is correct before connecting the motherboard to the power supply.
6. To prevent electric shock or damage, always turn off the AC power or unplug the power cord before removing or reconfiguring the motherboard or any components.
7. Unplug the AC power cord from the outlet before relocating the motherboard or any components.
8. Ensure all power cords are unplugged before connecting or disconnecting any equipment to avoid electrical hazards.
9. Wait at least 30 seconds after powering off the system before powering it on again to prevent unnecessary wear.
10. If any issues arise during operation, consult a qualified professional for assistance.
11. This product may cause radio interference in certain environments; if necessary, users should take appropriate measures to mitigate such interference.

# AL-35

# User Manual

(Version 1.2)

| Version: | | |
|---|---|---|
| NO. | Description | Issue Date: |
| V0.5 | Initial Version. | 2023/03/22 |
| V1.0 | 1. Change Intel i226 NIC to Intel i210<br>2. Change SODIMM-DDR5 to SODIMM-DDR4.<br>3. Modified the USB 2.0 pin/COM pin. | 2024/02/29 |
| V1.2 | 4. LVDS voltage switching changed from resistor switching to jumper switching. (Chinese Version) | 2024/09/02 |
| V1.2 | 4. English Version | 2025/07/14 |
| *Please Note:*<br>*The issue date on the Chinese version is the mass production date, while the English version shows the translation date.* | | |

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# Chapter 1 Product Introduction

## 1.1 Brief Introduction

The AL-35 motherboard is a 3.5" single board computer (SBC) based on the Intel® Alder Lake-U series platform. It features a compact form factor combined with high computing performance, making it ideal for energy-efficient applications.

## 1.2 Parameters

**Intel Alder Lake U Series:**

| CPU | Cores/Threads | Base Frequency | Max Turbo Frequency (P-core/ E-core) | Cache | TDP |
|---|---|---|---|---|---|
| Intel Core i7-1255U | 10C/12T | 1.7GHz | 2*P-Cores: 4.7 GHz/8*E-Cores: 3.5GHz) | 12MB | Processor Base Power: 15W, Maximum Turbo Power:55W. PL1/PL2:15W. (Configured at 15W by default. Both sustained (PL1) and boost (PL2) power limits are set to 15W.) |
| Intel Core i5-1235U | 10C/12T | 1.3GHz | 2*P-Cores: 4.4 GHz/8*E-Cores: 3.3GHz) | 12MB | Processor Base Power: 15W, Maximum Turbo Power:55W. PL1/PL2:15W. (Configured at 15W by default. Both sustained (PL1) and boost (PL2) power limits are set to 15W.) |
| Intel Core i3-1215U | 6C/8T | 1.2GHz | 2*P-Cores: 4.4 GHz/4*E-Cores: 3.3GHz) | 10MB | Processor Base Power: 15W, Maximum Turbo Power:55W. PL1/PL2:15W. (Configured at 15W by default. Both sustained (PL1) and boost (PL2) power limits are set to 15W.) |

**GPU**: Integrated Graphics based on CPU, display via 2x HDMI2.0b, 1x LVDs (eDP optional)

| | |
|---|---|
| Intel Core i7-1255U | Intel® Iris® Xe Graphics eligible. 96EU (Execution Units). Max Dynamic Frequency:1.25GHz |
| Intel Core i5-1235U | Intel® Iris® Xe Graphics eligible. 80EU (Execution Units). Max Dynamic Frequency:1.20GHz |
| Intel Core i3-1215U | Intel® UHD Graphics for 12th Gen Intel® Processors. 64EU (Execution Units). Max Dynamic Frequency:1.10GHz |

**Memory:** 2x SO-DIMM DDR4-3200MHz slots, supports dual channel, up to 64GB for maximum capacity.

**Storage**: 1xM.2 Key_M slot, supports 2280 SSDs NVMe protocols at PCIe X4 speed. 1x M.2 Key_B slot, supports 2242 SSDs SATA 3.0 protocols or 3042 4G modules. 1x SATA3.0 interface.

**USB:** 4x USB3.2 Gen 2 ports, 4x USB2.0 onboard headers.

**Ethernet:** Two Intel Gigabit Network Controllers, 1x Intel i210+1x Intel i219. Data Rate Per Port: 1.0Gbps

**Audio:** High-definition Realtek audio codec. Supports one CTIA 2-in-1 combo jack (Line-out and Mic-in), and one built-in stereo amplifier output for passive speaker connection.

**Serial I/O:** 6x RS232 COM headers. COM1 and COM2 can be configured as RS232/RS422/RS485 via BIOS. COM5 and COM6 are 3-wire RS232.

**Expansion:** 1x M.2_Key E Slot type 2230 for Wi-Fi and Bluetooth module (PCIE/USB2/CNVi).

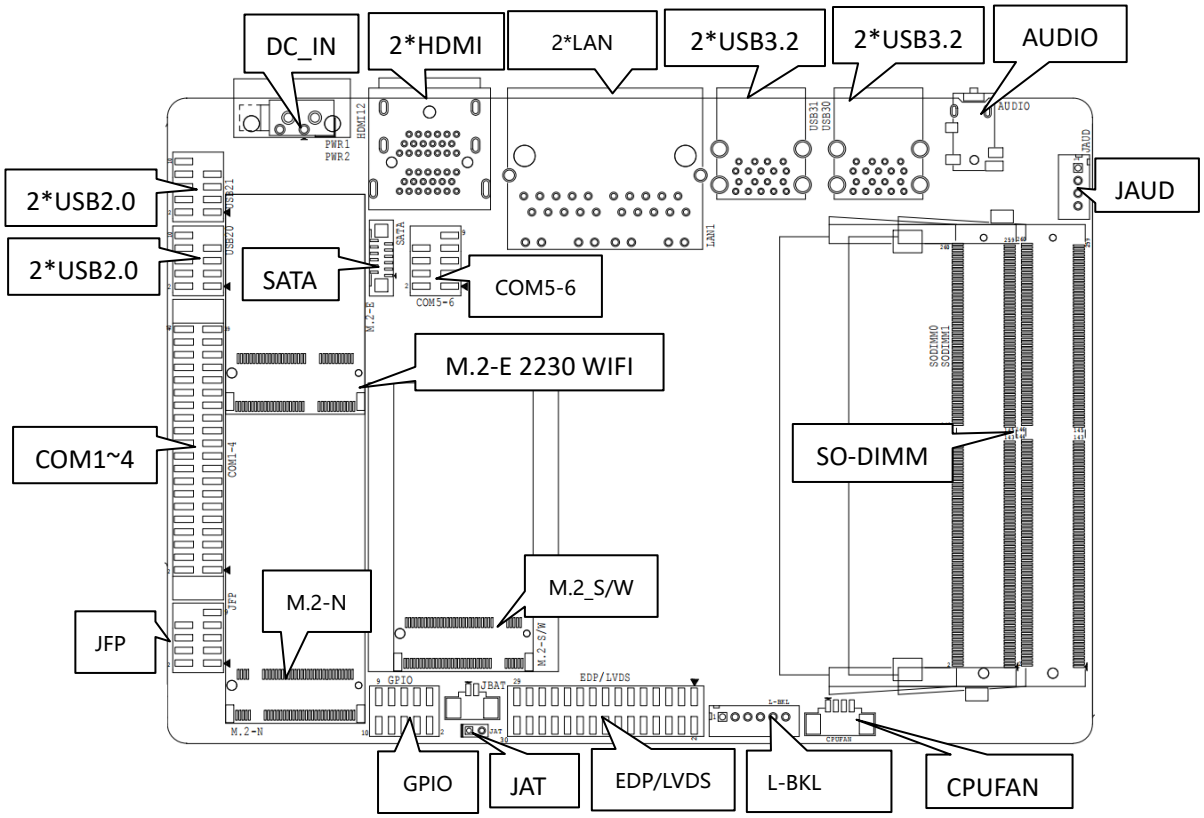
**Other I/O:** 1xSIM Card Slot, JFP, GPIO, CN1.

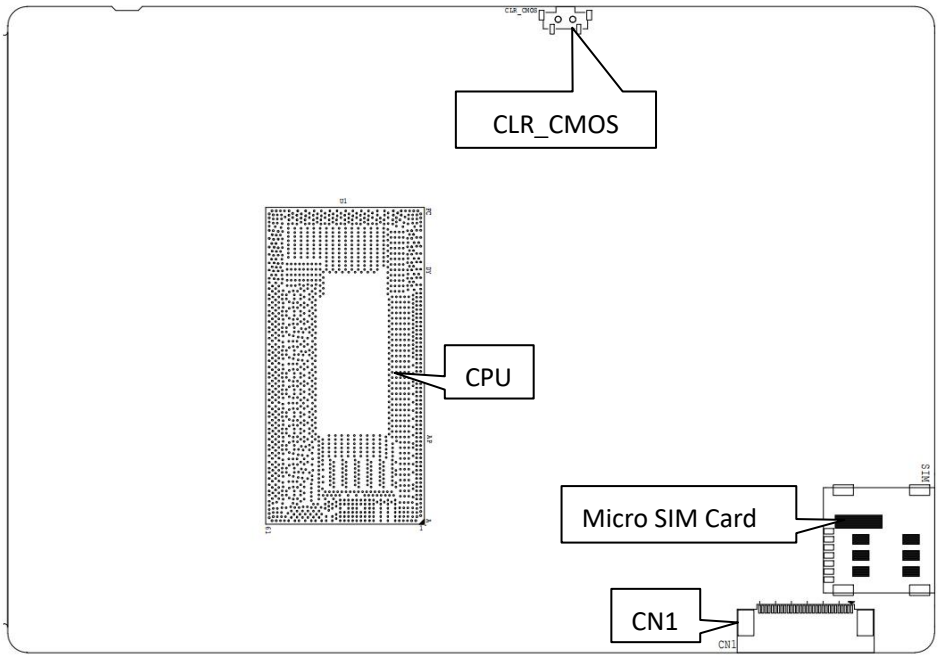
**Dimension:** 146mm x 102 mm

**Power:** 12V-35V. Supports wide voltage input from 12V to 35V via Phoenix terminal DC power adapter. (Please Note: When connecting to an LVDS or eDP display, a DC power adapter with a voltage of 19V or higher is required.)

**Working Temperature:** -20℃~60℃

## 1.3 Connector Diagram



# Chapter 2 Hardware

## 2.1 Installations

Please refer to the following steps for installations:

1. Read the user manual carefully to make sure all the adjustments on the AL-35 are correct.
2. Installing the Memory:
   - Press the ejector tab of the memory slot outwards with your fingertips.
   - Hold the memory module and align the key to the module with that on the memory slot.
   - Gently push the module into the slot until the ejector levers return completely to the closed position, holding the module in place when the module touches the bottom of the slot. To remove the module, press the ejector levers outwards to unseat the module.
3. Installing the expansion cards:
   - Locate the expansion slots and remove the screw, insert the cards into the slot at a 45-degree angle then attach the screw to the expansion cards, gently press down on it then install the screw back.
4. Connect all signal wires, cables, panel control wiring, and power supplies.
5. Start the computer and complete the setup of the BIOS program.

The board's components are integrated circuits and can easily be damaged by Electrostatic Discharge or ESD; therefore, please follow the instructions:

- Hold the board's edge when handing, and do not touch onboard pins, components, or plug sockets.
- When touching integrated circuit components (such as CPU, RAM, etc.), please wear an anti-static wrist strap/glove to avoid electrostatic discharge damage to the board or other sensitive components.
- Before installing the integrated circuits/sensitive components, place the sensitive components in anti-static bags to keep them safe from ESD.
- Please make sure the power switch is OFF before plugging the power plug.

## 2.2 Jumper Setting

Please configure the jumpers according to your requirements before installing the hardware.

How to identify the first header of jumpers and pins: Observe the mark beside the jumper or pins and find the header marked by “1” or bold line or triangular symbol. Or observe the rear panel and the header with a square solder pad is the first header.

## 2.3 Memory Slots

The board provide 2xSO-DIMM DDR4-3200MHz slots up to 64GB for maximum memory capacity.

Notes: Make sure to hold the memory module and align the key to the module with that on the memory slot. While choosing a memory module, please make sure the module matches the board’s specifications.

## 2.4 Display Interfaces (Screen Printing: HDMI12, EDP/LVDS)

The board features two HDMI2.0b interfaces (support HDCP2.3) for 4K resolution at 60Hz; and one 24bit LVDs interface (eDP optional) for resolution up to 1920x1080.

## 2.4.1 **LVDS** (Screen Printing: EDP/LVDS, L-BKL, L_VCC/BKL)

When it is configured as an LVDS function, the "EDP/LVDS" pin transmits LVDS signals, the “L-BKL” pin controls the backlight, and the “L_VCC/BKL” pin regulates the panel operating voltage and backlight forward polarity.

**LVDS Data Pin** (Screen printing: EDP/LVDS)

| Signal | Pin | | Signal |
|---|---|---|---|
| VCC | 1 | 2 | VCC |
| VCC | 3 | 4 | GND |
| GND | 5 | 6 | GND |
| A_DATA0_DN | 7 | 8 | A_DATA0_DP |
| A_DATA1_DN | 9 | 10 | A_DATA1_DP |
| A_DATA2_DN | 11 | 12 | A_DATA2_DP |
| GND | 13 | 14 | GND |
| A_CLK_DN | 15 | 16 | A_CLK_DP |
| A_DATA3_DN | 17 | 18 | A_DATA3_DP |
| B_DATA0_DN | 19 | 20 | B_DATA0_DP |
| B_DATA1_DN | 21 | 22 | B_DATA1_DP |
| B_DATA2_DN | 23 | 24 | B_DATA2_DP |
| GND | 25 | 26 | GND |
| B_CLK_DN | 27 | 28 | B_CLK_DP |
| B_DATA3_DN | 29 | 30 | B_DATA3_DP |

**LVDS Backlight Adjustment Pin** (Screen printing: L-BKL)

| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | LCD_BKL_ADJ |
| 4 | LCD_BKL_ON |
| 5 | 12V |
| 6 | 12V |

**LVDS Operating Voltage and Backlight Polarity Configuration Pin** (Screen printing: L_VCC/BKL)

| Interface | Jumper | Function |
|---|---|---|
| 1-3 | Close | VCC(+3.3V) |
| 3-5 | Close | VCC(+5V) |
| 2-4 | Close | REV(Backlight polarity: reverse) |
| 4-6 | Close | STD(Backlight polarity: forward) |

Please Note: The LVDS panel power supply is configurable via jumper, allowing flexible selection between 5V and 3.3V. Users should use jumper caps to short the pins corresponding to the required voltage based on the LVDS panel specifications. Warning: Do not short pins for different voltages simultaneously, as this may damage the board or connected components.

## 2.4.2 eDP (Optional)

When it is configured as an eDP function, the "EDP/LVDS" pin transmits eDP signals, the “L-BKL” pin controls the backlight, and the “L_VCC/BKL” pin regulates the panel operating voltage and backlight forward polarity.

**eDP Data Pin** (Screen printing: EDP/LVDS)

| Signal | Pin | | Signal |
|---|---|---|---|
| VCC | 1 | 2 | VCC |
| VCC | 3 | 4 | EDP_HPD |
| GND | 5 | 6 | GND |
| EDP_AUXN | 7 | 8 | EDP_AUXP |
| N/A | 9 | 10 | N/A |
| EDP_DATA0_P | 11 | 12 | EDP_DATA0_N |
| GND | 13 | 14 | GND |
| N/A | 15 | 16 | N/A |
| EDP_DATA1_P | 17 | 18 | EDP_DATA1_N |
| N/A | 19 | 20 | N/A |
| N/A | 21 | 22 | N/A |
| N/A | 23 | 24 | N/A |
| GND | 25 | 26 | GND |
| N/A | 27 | 28 | N/A |
| N/A | 29 | 30 | N/A |

**eDP Backlight Adjustment Pin** (Screen printing: L-BKL)

| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | LCD_BKL_ADJ |
| 4 | LCD_BKL_ON |
| 5 | 12V |
| 6 | 12V |

**eDP Operating Voltage and Backlight Polarity Configuration Pin** (Screen printing: L_VCC/BKL)

| Interface | Jumper | Function |
|---|---|---|
| 1-3 | Close | VCC(+3.3V) |
| 3-5 | Close | VCC(+5V) |
| 2-4 | Close | REV(Backlight polarity: reverse) |
| 4-6 | Close | STD(Backlight polarity: forward) |

Please Note: The eDP panel power supply is configurable via jumper, allowing selection between 5V and 3.3V. Warning: Do not short pins for different voltages simultaneously, as this may damage the board or connected components.

## 2.5 Storage Interfaces

The board provides 1xM.2 Key M 2280 slot (PCIe4.0 X4 Signal) for NVMe SSD, 1x SATA3.0 FPC interface, 1xM.2 key B 2242 Slot for SATA SSD or 3042 4G module with SIM card slot.

**FPC SATA Definition** (Screen Printing: SATA)

| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | TX_N |
| 3 | TX_P |
| 4 | GND |
| 5 | RX_P |
| 6 | RX_N |
| 7 | GND |
| 8 | +5V |
| 9 | +5V |
| 10 | +5V |
| 11 | GND |
| 12 | GND |

## 2.6 Expansion Slots

The board features 1x M.2_Key E 2230 slot for Wi-Fi and Bluetooth Modules (supports PCIe/USB2/CNVi).

## 2.7 USB Interfaces

The board supports 4x USB 3.2 Gen2 rear ports and 4x USB 2.0 internal headers (2.0mm pitch).

**Internal USB2.0 Pin** (Screen Printing: USB20, USB21)

| Signal | Pin | | Signal |
|---|---|---|---|
| VCC 5V | 1 | 2 | VCC 5V |
| USB DATA- | 3 | 4 | USB DATA- |
| USB DATA+ | 5 | 6 | USB DATA+ |
| GND | 7 | 8 | GND |
| NC | 9 | 10 | (NULL) |

## 2.8 LAN

The board features 2xRJ45 LANs interfaces with high-speed Intel network controllers (1x Intel i210+1x Intel i219), data rate per ports: 1.0Gbps. Both of the Ethernet interfaces supports network wake-up (Magic packet wake-up), and the LAN1 supports UEFI PXE network boot.

**LED Status Indicators:**

| LI_LED Status (Green) | Function | ACT_LED Status (Orange) | Function |
|---|---|---|---|
| Always on | Network Connected | Flashing | Data Transmission |

## 2.9 COM

The board features built-in 2.0 mm pitch serial headers and supports 6x RS232 serial ports by default. COM1 and COM2 can be configured as RS232, RS485, or RS422 via BIOS settings. COM5 and COM6 are 3-wire RS232. Additionally, the 10th pin of each serial port header from COM1 to COM4 provides 12V power output.

**RS232 COM** (Screen Printing: COM14)

| Signal | Pin | | Singal |
|---|---|---|---|
| DCD# | 1 | 2 | RXD |
| TXD | 3 | 4 | DTR# |
| GND | 5 | 6 | DSR# |
| RTS# | 7 | 8 | CTS# |
| RI# | 9 | 10 | +12V |
| DCD# | 11 | 12 | RXD |
| TXD | 13 | 14 | DTR# |
| GND | 15 | 16 | DSR# |
| RTS# | 17 | 18 | CTS# |
| RI# | 19 | 20 | +12V |
| DCD# | 21 | 22 | RXD |
| TXD | 23 | 24 | DTR# |
| GND | 25 | 26 | DSR# |
| RTS# | 27 | 28 | CTS# |
| RI# | 29 | 30 | +12V |
| DCD# | 31 | 32 | RXD |
| TXD | 33 | 34 | DTR# |
| GND | 35 | 36 | DSR# |
| RTS# | 37 | 38 | CTS# |
| RI# | 39 | 40 | +12V |

**COM5_6 Default Definition RS232** (Screen: COM5_6)

| Singal | Pin | | Signal |
|---|---|---|---|
| NC | 1 | 2 | NC |
| RX5 | 3 | 4 | RX6 |
| GND | 5 | 6 | GND |
| TX5 | 7 | 8 | TX6 |
| NC | 9 | 10 | (NC) |

**COM1, COM2 Optional Definition RS232/RS485/RS422**

| Pin | RS232 | RS485 | RS422 |
|---|---|---|---|
| 1 | DCD | DATA- | TX- |
| 2 | RXD | DATA+ | TX+ |
| 3 | TXD | (NC) | RX+ |
| 4 | DTR | (NC) | RX- |
| 5 | GND | GND | GND |
| 6 | DSR | (NC) | (NC) |
| 7 | RTS | (NC) | (NC) |
| 8 | CTS | (NC) | (NC) |
| 9 | RI | (NC) | (NC) |

## 2.10 **GPIO** (Screen Printing: GPIO)

The board provides a 2×5-pin GPIO header (2.0 mm pitch), offering 8 programmable general-purpose input/output (GPIO) ports.

**GPIO** (Screen Printing: GPIO)

| Signal | Pin | | Signal |
|---|---|---|---|
| SIO_GP70 | 1 | 2 | 3.3V |
| SIO_GP71 | 3 | 4 | SIO_GP74 |
| SIO_GP72 | 5 | 6 | SIO_GP75 |
| SIO_GP73 | 7 | 8 | SIO_GP76 |
| GND | 9 | 10 | SIO_GP77 |

Note: For detailed information on the GPIO_WD0 configuration file, please refer to the appendix.

## 2.11 **Board Power Supply** (Screen printing: PWR1, PWR2)

The board provides a 2-Pin DC-IN phoenix connector that supports 12V-35V input for power supply.

**PWR1** (Screen Printing: PWR1)

| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | VCC |

**PWR2** Optional Socket (Screen Printing: PWR2)

| Pin | Signal |
|---|---|
| 1 | VCC |
| 2 | VCC |
| 3 | GND |
| 4 | GND |

## 2.12 Switch Button/Light Indicator (Screen Printing: JFP)

The board has a set of 2.0mm spacing pins that can be connected to a switch button, a system reset button, a hard disk read/write indicator, and a power-on indicator.

**Switch Button/Light Indicator Pin Definition** (Screen Printing: JFP)

| Signal | Pin | | Signal |
|---|---|---|---|
| HDD_LED+ | 1 | 2 | PWR_LED+ |
| HDD_LED- | 3 | 4 | PWR_LED- |
| RSTBTN- | 5 | 6 | PWR_ON+ |
| RSTBTN+ | 7 | 8 | PWR_ON- |
| NC | 9 | 10 | (NC) |

## 2.13 Audio Interface

The board features a Realtek ALC897 audio codec, supports a 3.5mm Line-out/MIC two-in-one combo jack (CTIA American standard), and a built-in dual-channel power amplifier output socket for connecting passive speakers.

**Two-in-one headphone jack**:




**JAUD** (Screen Printing: JAUD)

| Pin | Signal |
|---|---|
| 1 | L+ |
| 2 | L- |
| 3 | R- |
| 4 | R+ |

## 2.14 CPU Fan (Screen printing: CPUFAN)

The board features one auxiliary CPU cooling fan header, providing a default 5V power supply, with an optional 12V configuration available.

**CPUFAN** (Screen Printing: CPUFAN)

| Pin | Signal |
|---|---|
| 1 | VCC |
| 2 | GND |
| 3 | TAC |
| 4 | CTL |

## 2.15 Hardware Auto Start (Screen Printing: JAT)

The board includes a JAT header (2.0 mm pitch) to support hardware-based auto-start functionality, enabling automatic system boot upon power connection.

**JAT** (Screen Printing: JAT)

| Setting | JAT |
|---|---|
| Close | Hardware Auto Start |

## 2.16 CMOS Clearance/Retention (Screen printing: CLR_CMOS)

CMOS is powered by onboard button batteries. Clearing CMOS will permanently remove the previous system settings and restore the board system to original settings (factory settings).

**Step 1:** Turn off the PC and disconnect the power.

**Step 2:** Press CLR_CMOS for 15 seconds then disconnect.

**Step 3:** Restart the device, press the <DEL> button to enter the BIOS, load the optimal default value, save, and exit the settings.

⚠ ATTENTION: Please do not clear COMS when the PC is connected to power in case board damages.

# Chapter 3 BIOS Setup

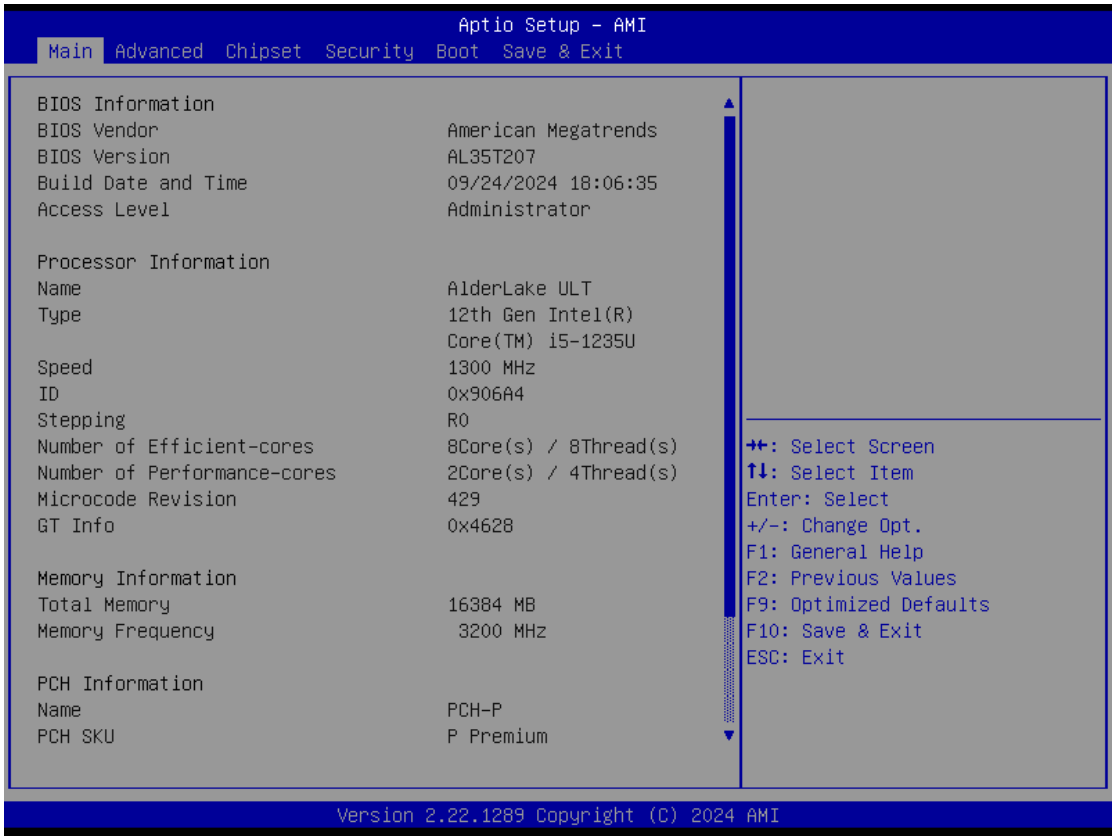
## 3.1 Entering the BIOS

1. Power on the computer and press the <Delete> key during startup to enter the BIOS setup utility.
2. BIOS Hotkey Functions

| Key | Function | Description |
|---|---|---|
| →← | Select Screen | Navigate between menu screens. |
| ↑↓ | Select Item | Move between menu items or options. |
| Enter | Select | Open a submenu or confirm a selection. |
| +/- | Change Option | Adjust values or change settings. |
| F1 | General Help | Display help information for the selected item. |
| F2 | Previous Values | Load the previously saved settings. |
| F9 | Optimized Defaults | Restore factory default settings. |
| F10 | Save & Exit | Save changes and exit BIOS. |
| ESC | Exit | Exit BIOS or return to the previous menu. |

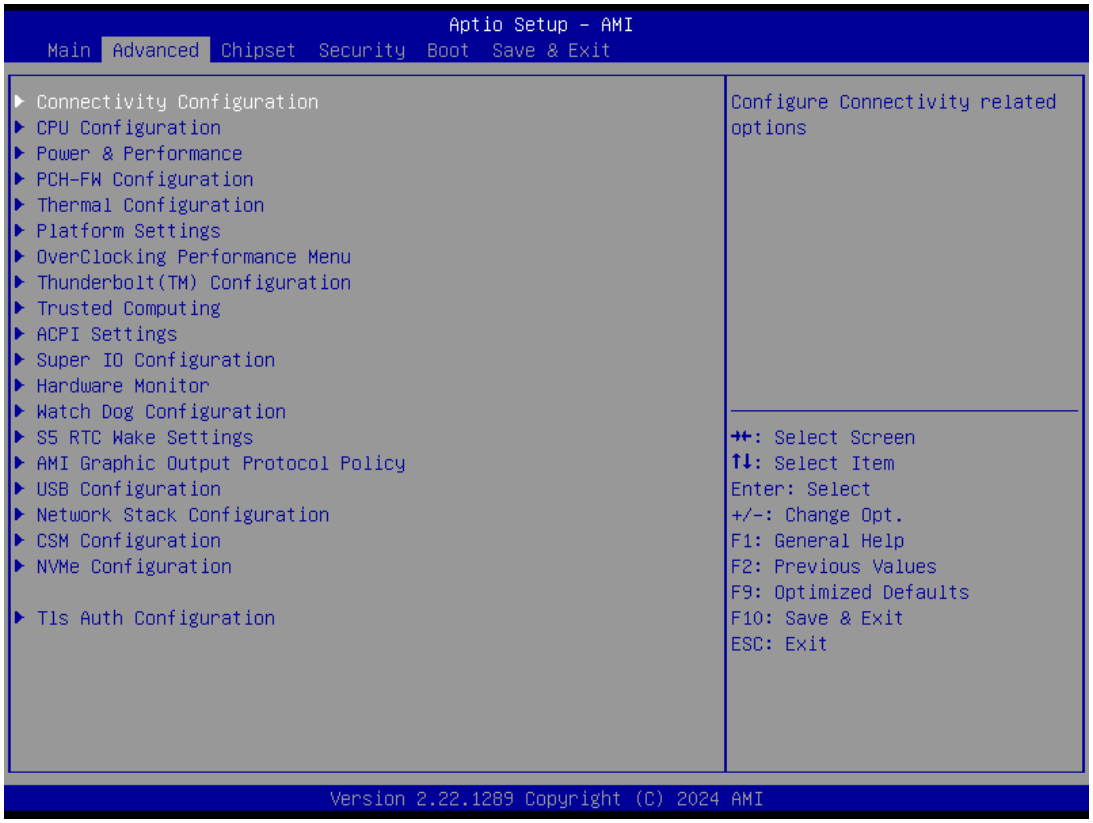
## 3.2 Main Setup (BIOS info, Date, Time）

When you enter the BIOS Setup utility the first things you will encounter is the Main Setup screen. Shown below is the Main BIOS Setup screen. You can always return to the Main setup by selecting the Main tab.




**BIOS Vendor**: American Megatrends
**BIOS Version**: Current BIOS version
**Build Date and Time**: BIOS build date and time
**Processor Information**: CPU model and speed
**Total Memory**: Installed system memory
**Memory Frequency**: Operating memory speed
**ME FW Version**: Management Engine firmware version
**System Date**: Set system date (MM/DD/YYYY)
**System Time**: Set system time (HH:MM:SS)

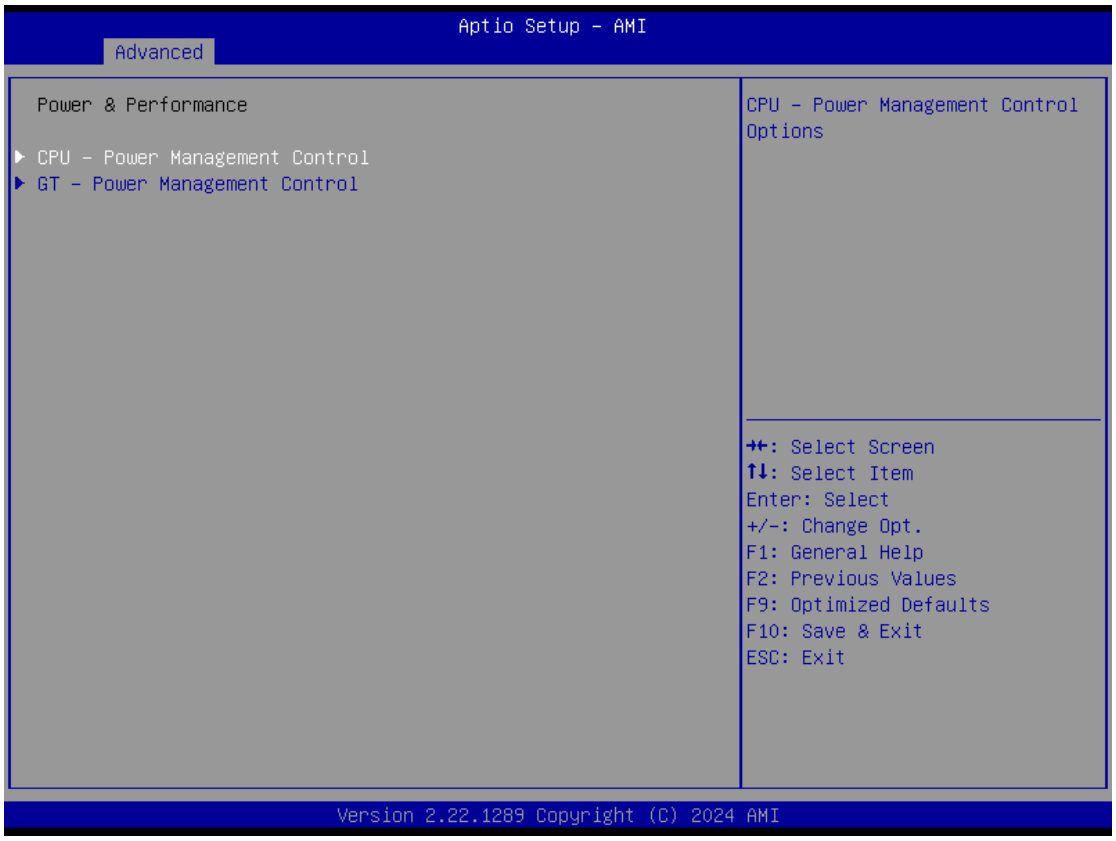
## 3.3 Advanced Settings




Select any of the items in the left frame of the screen. The advanced sections allow you to configure, improve and set up system features according to the preference of the CPU Configuration. All Advanced BIOS Setup options are described as follows.

1. Connectivity Configuration: Configure connection-related settings.
2. CPU Configuration: CPU Parameter Information and Common Settings Selection
3. Power & Configuration: Set power-related features and options.
4. Thermal Configuration: Monitor and configure thermal controls
5. Platform Settings: Platform-specific configuration options
6. Overclocking Performance Menu: Adjust overclocking settings (if supported)
7. Thunderbolt (TM) Configuration: *Not supported on this board.*
8. Trusted Computing: Manage trusted computing features.
9. ACPI Setting: Configure ACPI power management.
10. Super IO Configuration: Settings for legacy I/O devices.
11. Hardware Monitor: Monitor system voltages, temperatures, and fan speeds.
12. Watchdog Configuration: Watchdog Configuration.
13. S5 RTC Wake Settings: S5 RTC Wake Settings.
14. AMI Graphic Output Protocol Policy: AMI Graphic Output Protocol Policy
15. USB Configuration: Manage USB ports and functions.
16. Network Stack Configuration: Configure network boot options.
17. CSM Configuration: Set up Compatibility Support Module settings.
18. NVMe Configuration: View and manage NVMe devices.
19. Tls Auth Configuration: Configure TLS authentication options.

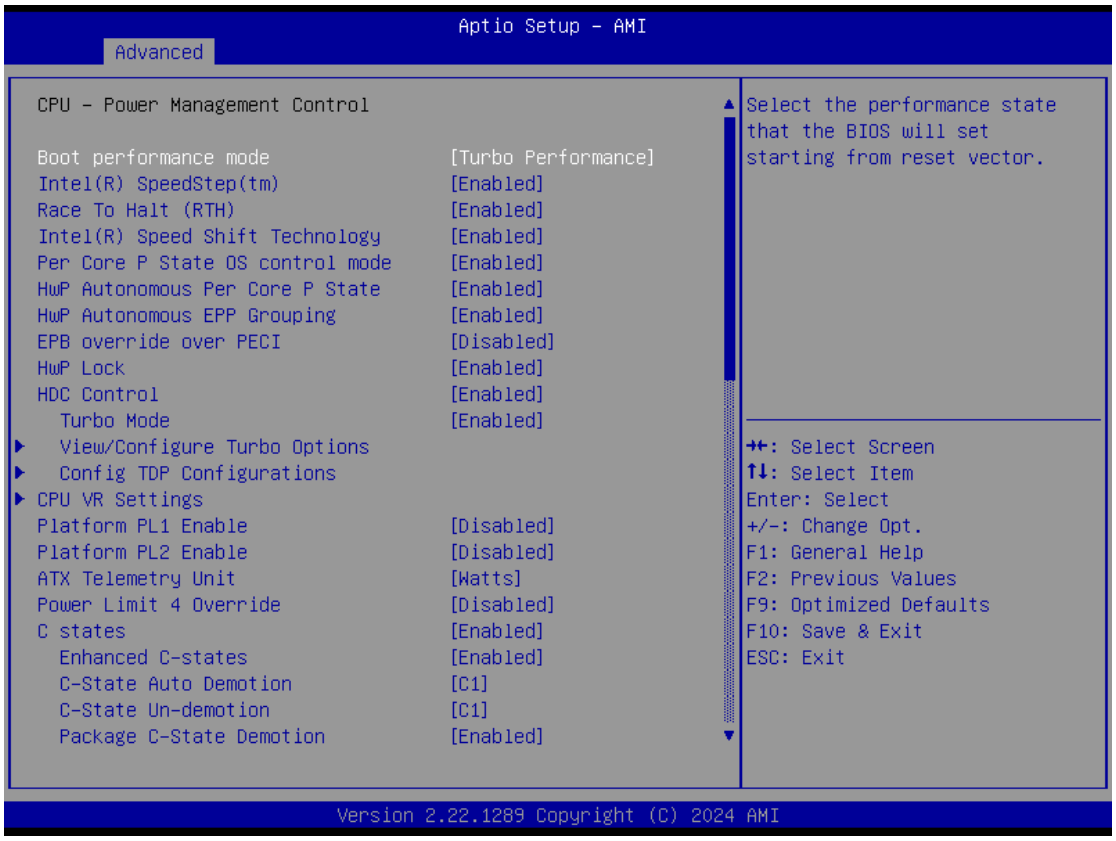
## 3.3.1 Power & Performance




**CPU-Power Management Control**

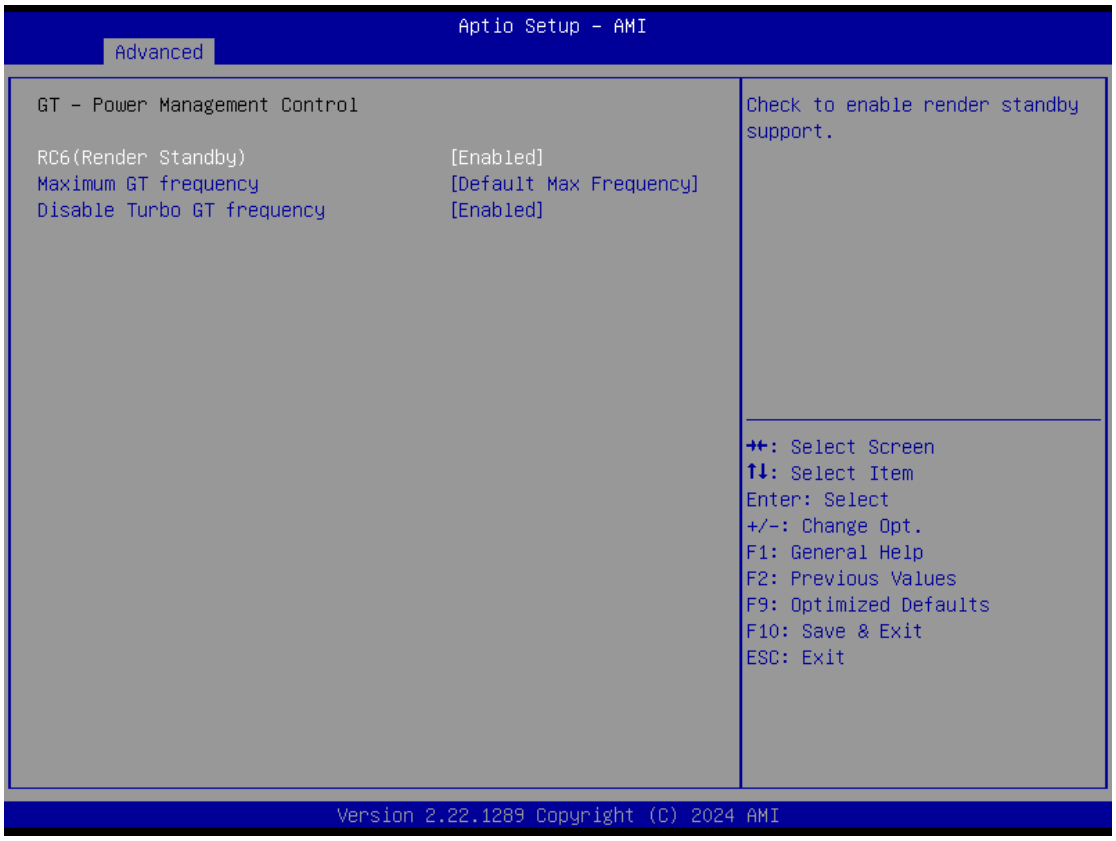
**GT-Power Management Control**

## 3.3.2 CPU-Power Management Control




1. **Boot Performance Mode:** Default Turbo Performance, Users can configure it to Maximum Battery Mode or Maximum Non-Turbo Performance Mode, depending on power and performance requirements.
2. **Intel® SpeedStep®(TM):** Enhanced Intel SpeedStep® Technology enables the operating system to control multiple frequencies and voltage points for optimal performance and power efficiency.
3. **Intel® Speed Shift Technology:** An energy-efficient frequency control method by the hardware rather than relying on OS control. Processor decision is based on the different system constraints for example Workload demand, and thermal limits while taking into consideration the minimum and maximum levels and activity window of performance requested by the operating system. Default “Enabled”.
4. **Turbo Mode:** The Turbo mode refers to Nehalem’s “Integrated Power Gate” power management technology, which allows running off some cores and adding power to the others so that they run at a higher frequency. The capacity of the entire CPU remains unchanged, and the efficiency of the CPU is optimized. Default “Enabled”.
5. **C states:** Idle States (C-states) are used to save power when the processor is idle. C0 is the operational state, meaning that the CPU is doing useful work 100% load. C1 is the first idle state, C2 the second, and so on, where more power-saving actions are taken for numerically higher C-states. C1 to C3 cuts off the clock inside the CPU, and C4 to C6 reduces the CPU voltage. Default “Enabled”.
6. **Enhanced C states:** C1 to C3 cuts the clock inside the CPU. C4 and C6 mode reduces CPU voltage. Features two way “Enhanced” mode, “Enabled” by default.

## 3.3.3 GT-Power Management Control




**RC6(Render Standby)：**

(Standby)Enable/disable integrated graphics standby, default Enabled.

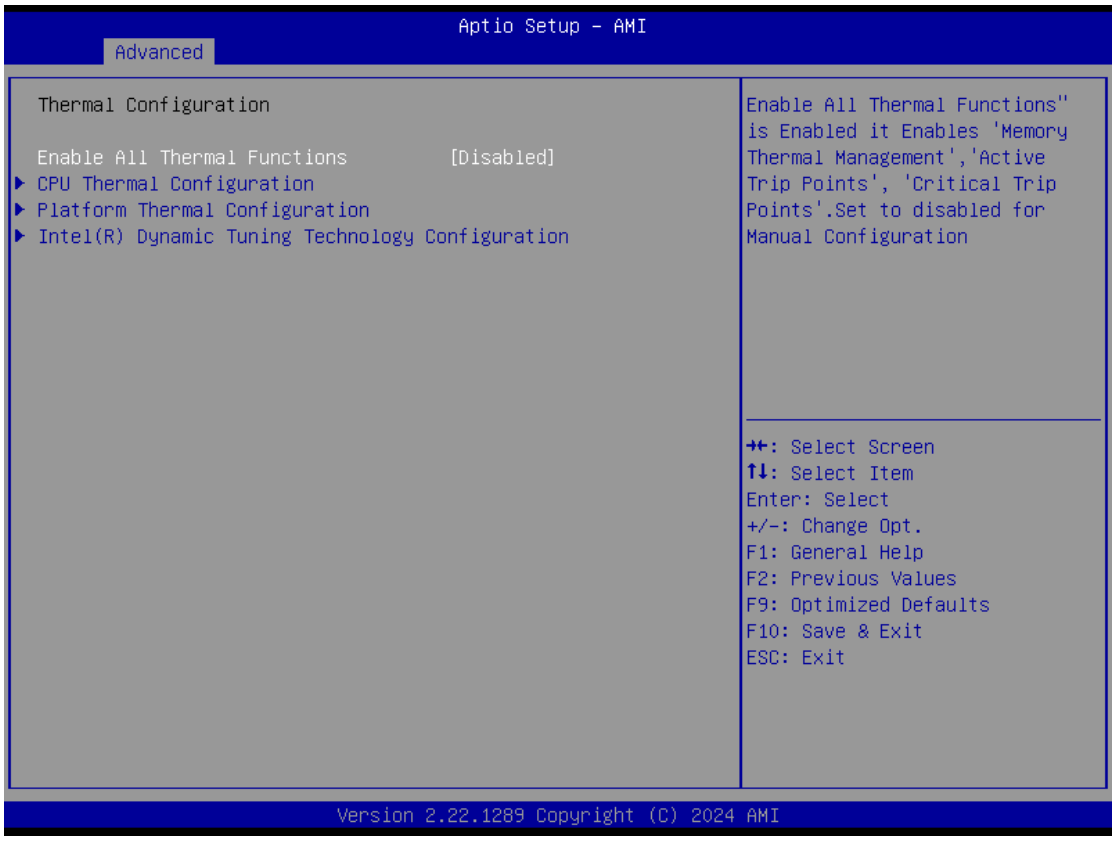
**Maximum GT frequency：**

Maximum GT Frequency, Default max frequency.

**Disable Turbo GT frequency：**

Disable Turbo GT Frequency mode, Default "Enabled".

## 3.3.4 Thermal Configuration




**Enable All Thermal Functions**

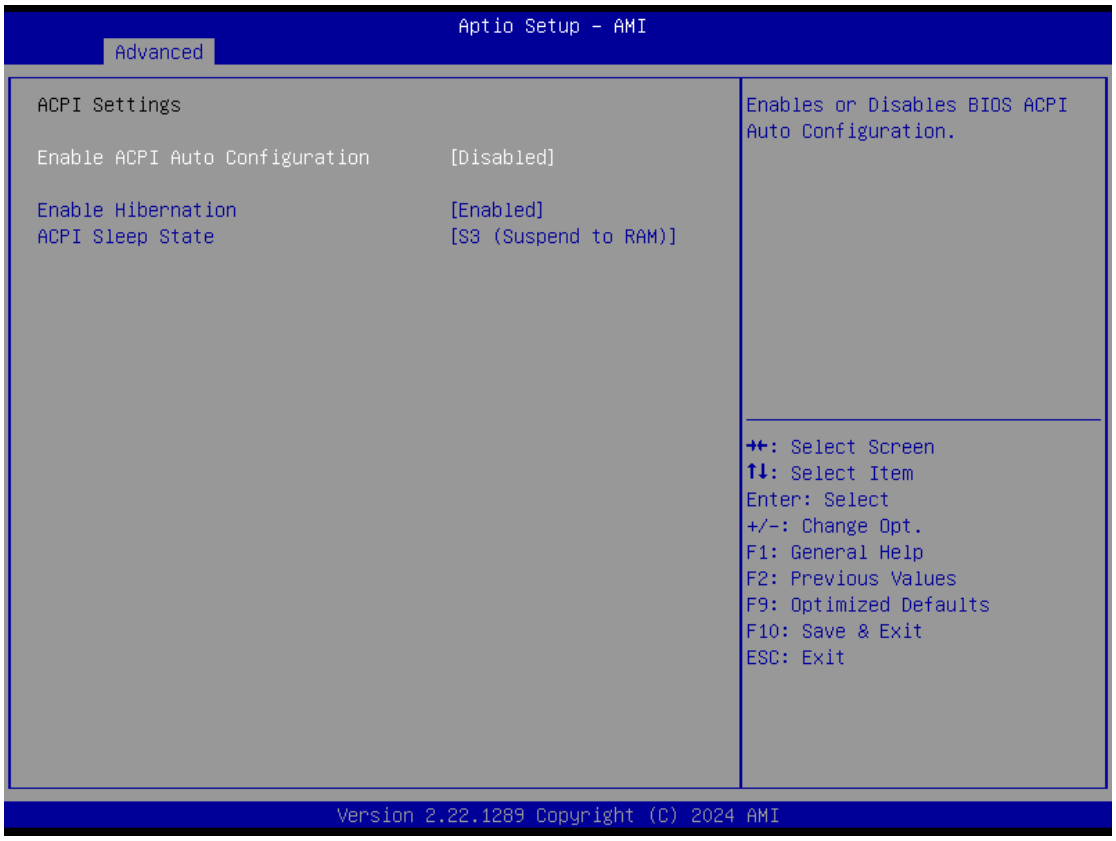
**CPU Thermal Configuration:**

Unlocks the temperature setting, the “Tcc Activation Offset” is the temperature adjustment option, the highest temperature is 100°C. Change the temperature by minus the number of degrees you wish to change. For example, minus 0(100-0) to set the temperature at 100°C, minus 20(100-20) to set the temperature at 80°C. (Please note the maximum supported temperature for the processor can be found on ark.intel.com.)

**Platform Thermal Configuration**

**Intel(R) Dynamic Tuning Technology Configuration**

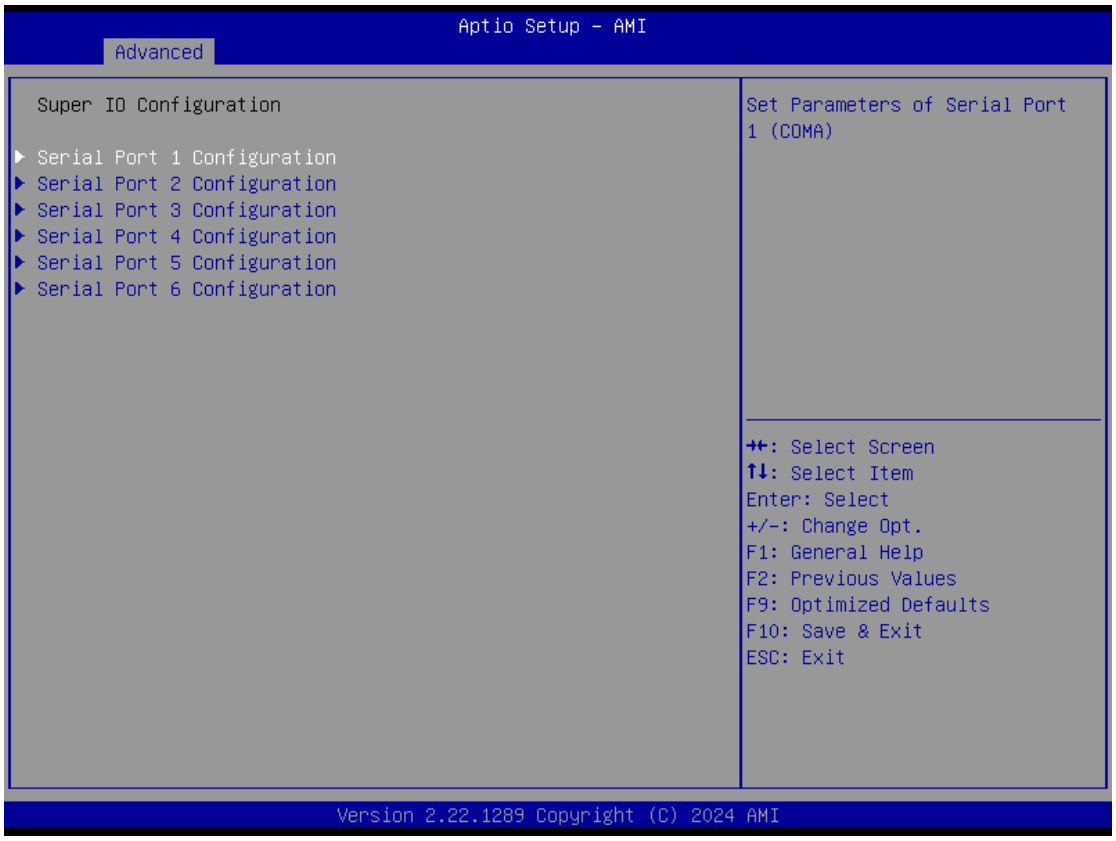
## 3.3.5 ACPI Setting




1. **Enabled ACPI Auto Configuration:** Enabled ACPI Auto Configuration, Default “Disabled”.
2. **Enabled Hibernation**
3. **ACPI Sleep State:**

   Configures ACPI power-saving modes in conjunction with the operating system to set different sleep functions.

## 3.3.6 Super IO Configuration



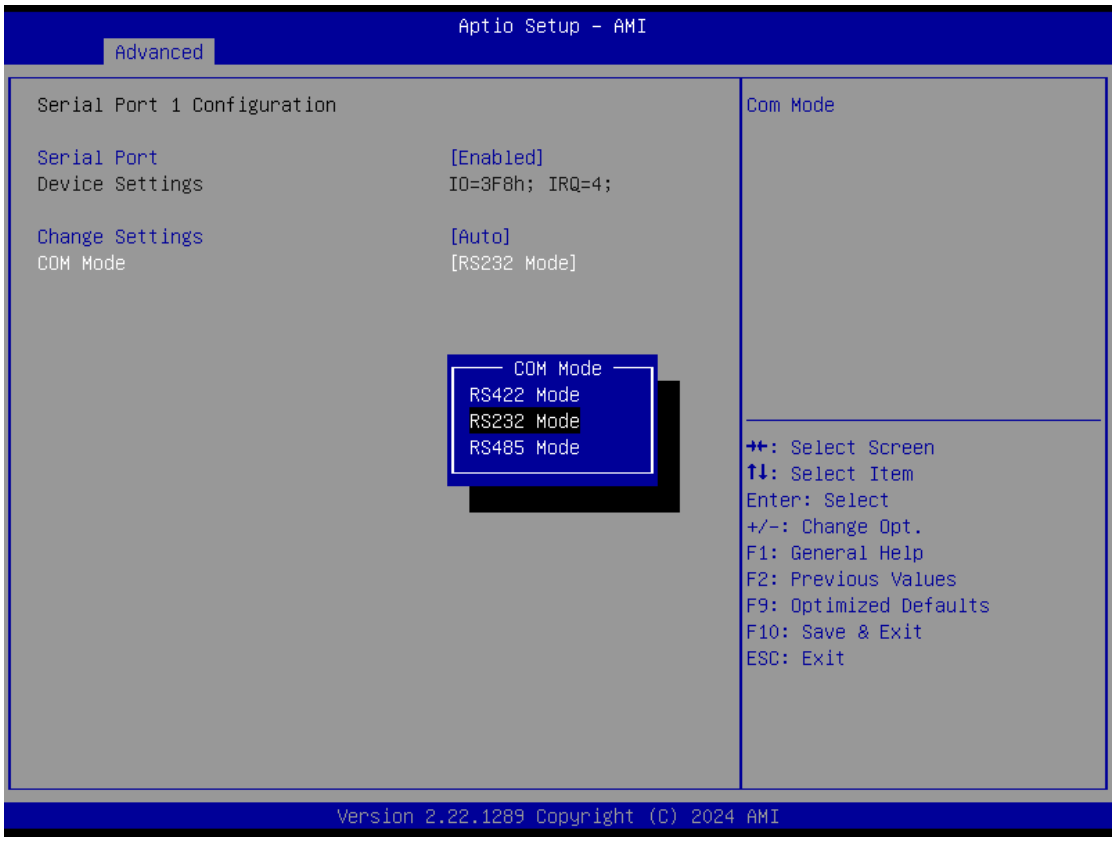

**Serial Port 1~6 Configuration**

**Serial Port:** Enable or disable serial port (COM).

**Device Setting (Read-only):** Displays serial ports' interrupt and location.

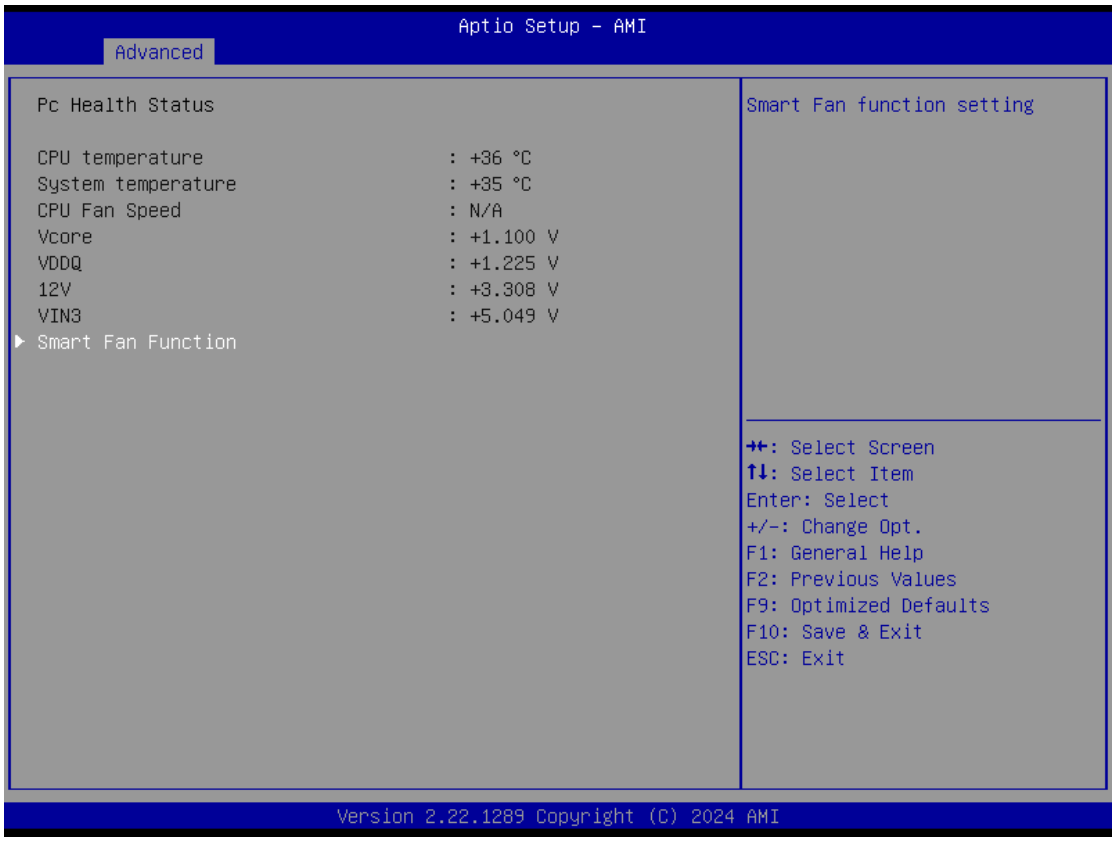
**Change Setting:** Change serial port settings and default setting is recommended as "Auto".

## 3.3.7 COM1, COM2 Protocols Switching (RS232/RS485/RS422)




To switch communication protocols, enter Serial Port 1/2 Configuration, locate the COM Mode option, and select the desired protocol: RS232, RS485, or RS422. The default setting is RS232.

## 3.3.8 Hardware Monitor

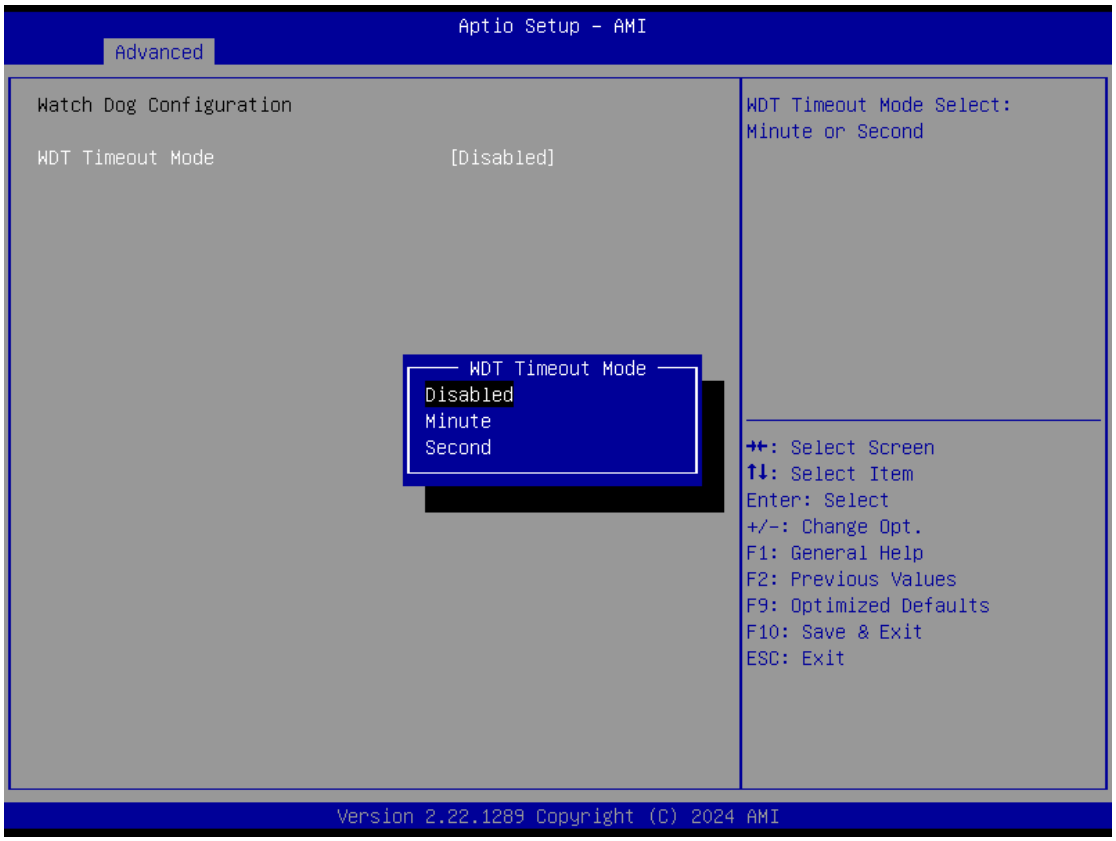



**PC Health Status**

The PC health status displays CPU temperature, system temperature, fan speed, and other relevant voltage values. The above parameters have a certain range, and the system cannot run beyond these ranges.

1. CPU Temperature
2. System Temperature
3. CPU Fan Speed: N/A
4. VCore: +1.100V (CPU core voltage)
5. VDDQ: +1.225V (RAM voltage)
6. 12V: +3.308V (Power Supply voltage, 12V power rail)
7. VIN3: +5.049V (Storage devices and USB ports voltage, 5V power rail)
8. Smart Fan Funtion
    i. Automatic Mode
    ii. Full on Mode
    iii. Manual Mode

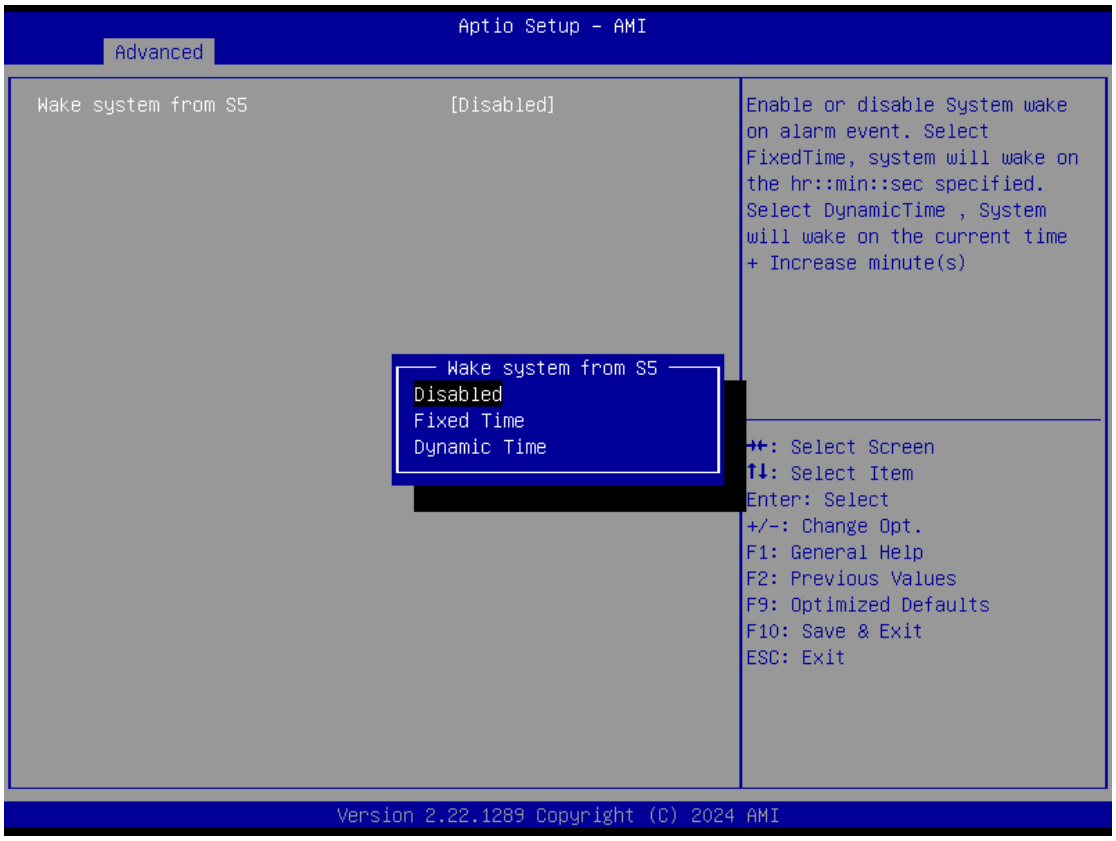
## 3.3.9 Watch Dog Configuration




**Watch Dog Configuration**

WDT Timeout Mode select: Minute or Second

## 3.3.10 S5 RTC Wake Settings

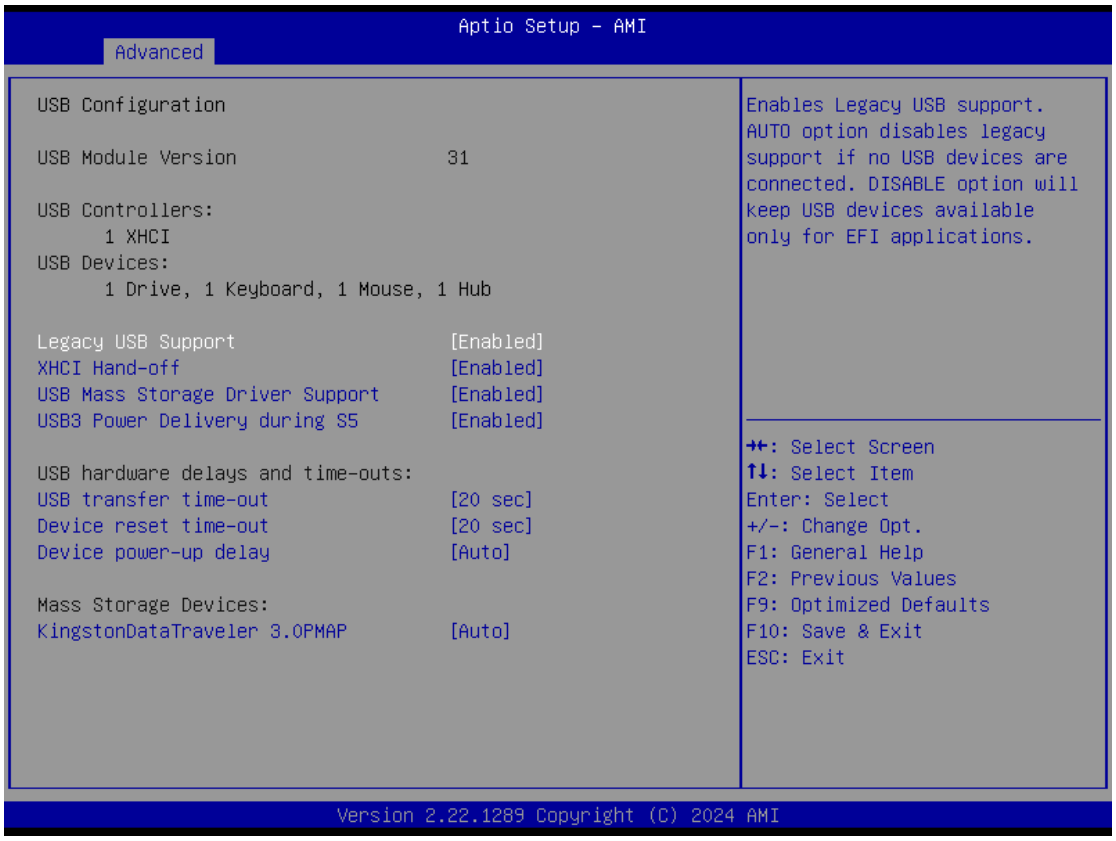



**Wake system From S5**: Allows the system to power on automatically from an S5 state. Disabled by default.

**Fixed Time:** Select Fixed Time and the system will wake on the Hr: Min: Sec specified.

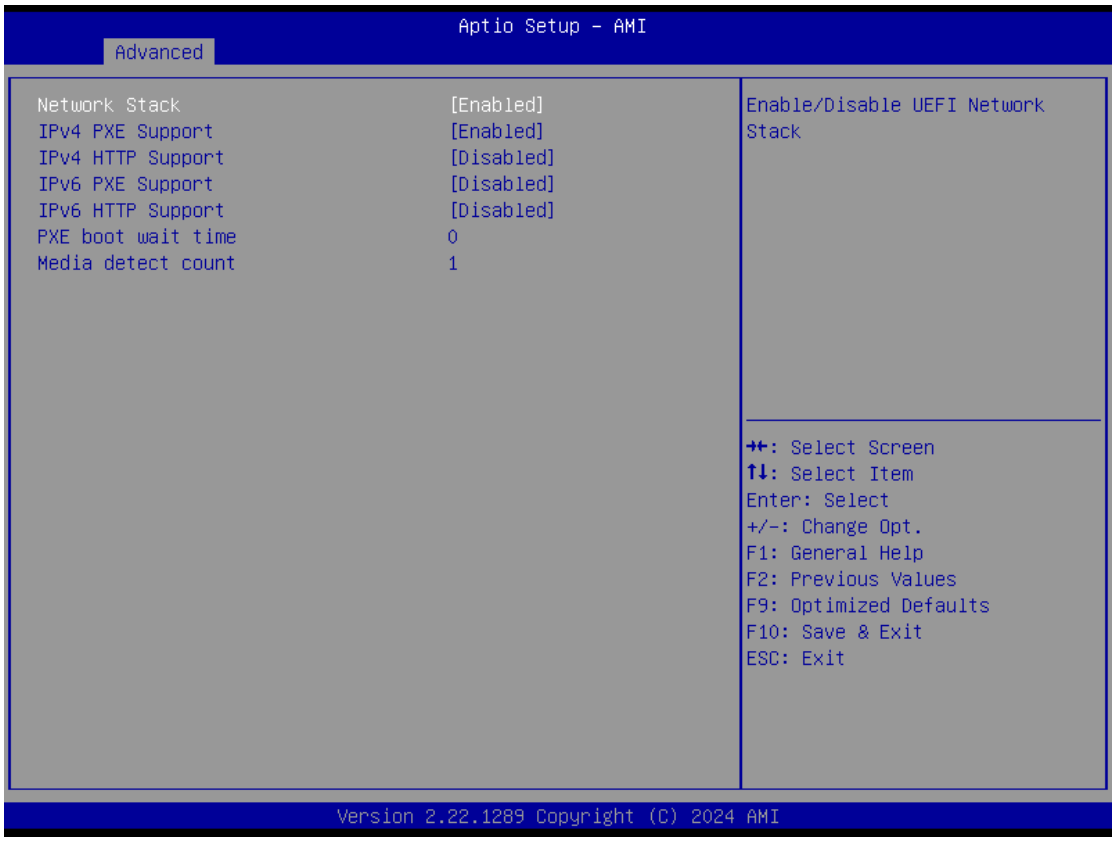
**Dynamic Time:** Select Dynamic Time and the system will wake on a dynamic time.

## 3.3.11 USB Configuration




1. **Legacy USB Support**
   a) Enable Legacy USB support. Disables legacy support if no USB devices are connected. Select enable will keep USB devices available under UEFI's support.
2. **XHCI Hand-off**
   a) A workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the USB XCHI driver.
3. **USB Mass Storage Driver Support**
   a) Enable(default) or disable USB Mass Storage Driver Support.
4. **USB transfer time-out**
   a) Sets the timeout for control, bulk, and interrupt transfers, default: 20 second.
5. **Device reset time-out**
   a) Defines the timeout for USB mass storage device start-up, default: 20 second.
6. **Device Power-up Delay**
   a) Specifies the maximum time a USB device may take to report itself to the host controller.

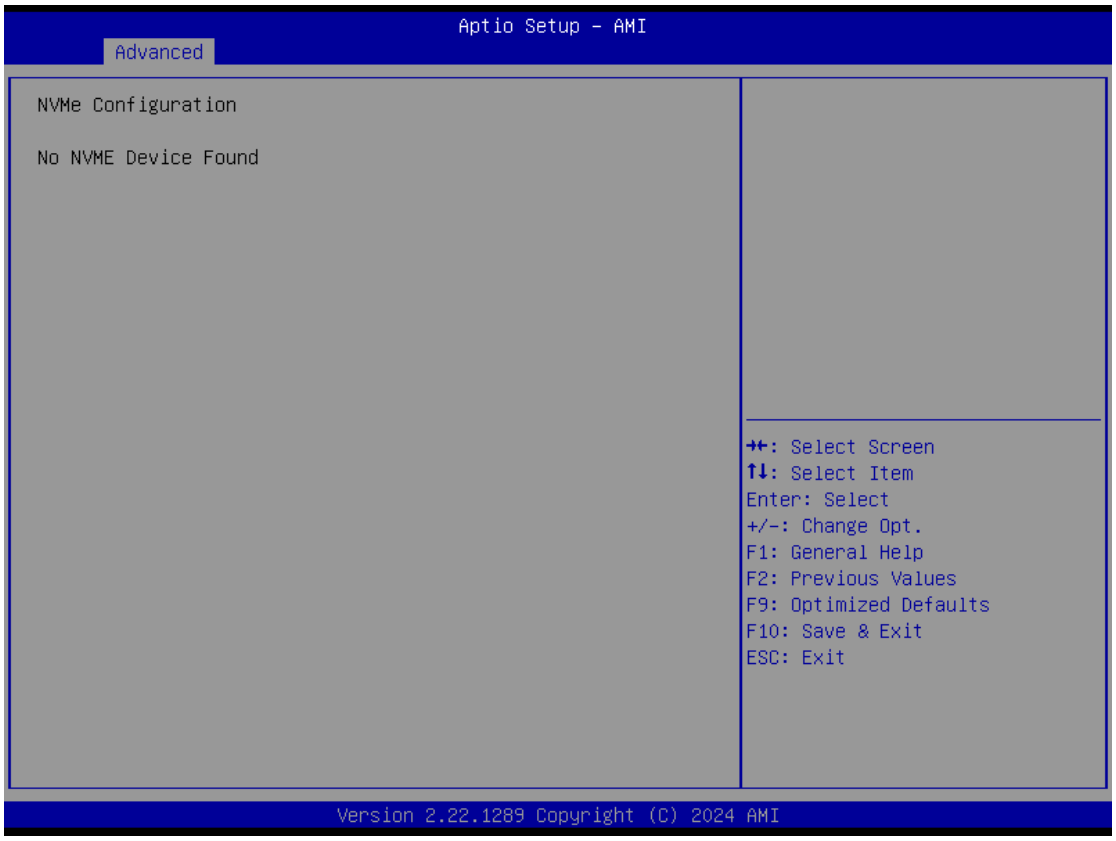
## 3.3.12 Network Stack Configuration




**Network Stack**

PXE Network boot setting, disabled by default.

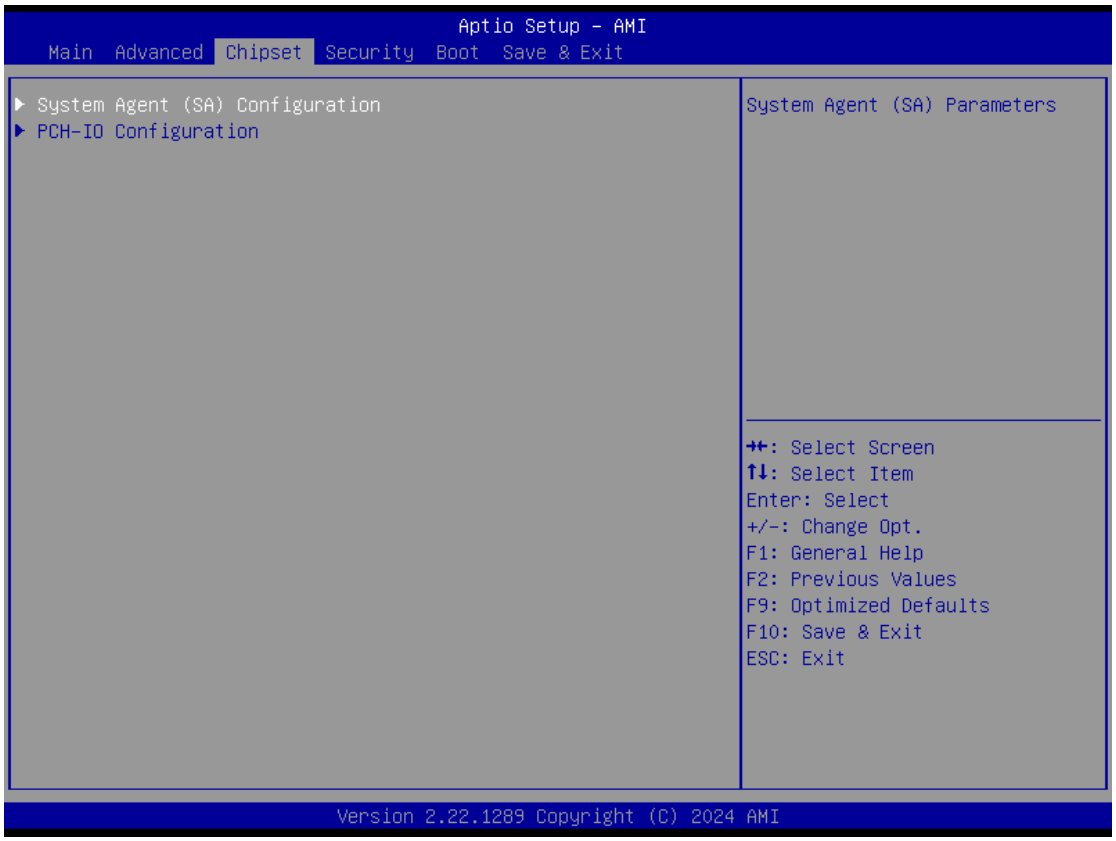
## 3.3.12 NVME Configuration




The capacity and model of the SSD will be displayed under the option after the NVMe protocol SSD has been installed.

## 3.4 Chipset

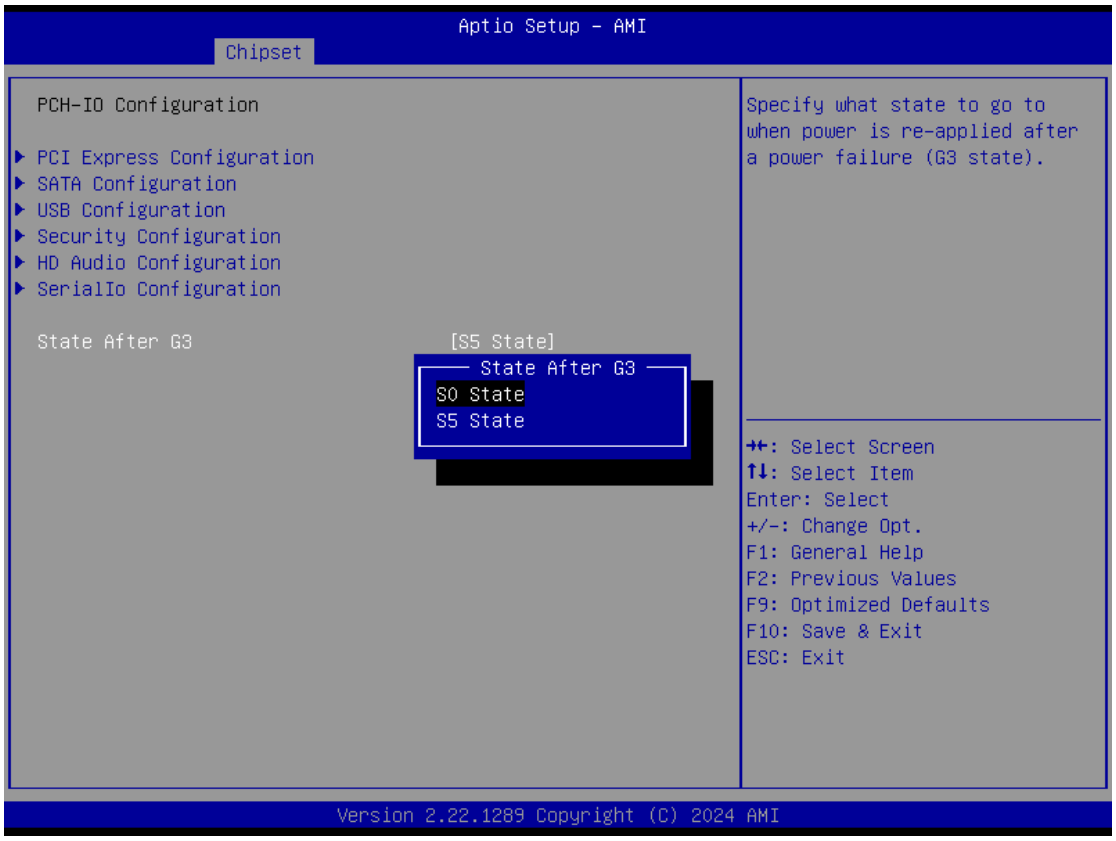
Select the chipset tab from the setup screen to enter the chipset BIOS Setup screen.




**System Agent (SA) Configuration:** Northbridge configuration options, including video memory, display devices, and other options.

**PCH-IO Configuration:** Southbridge configuration options, including hard disk, sound card equipment, and other options

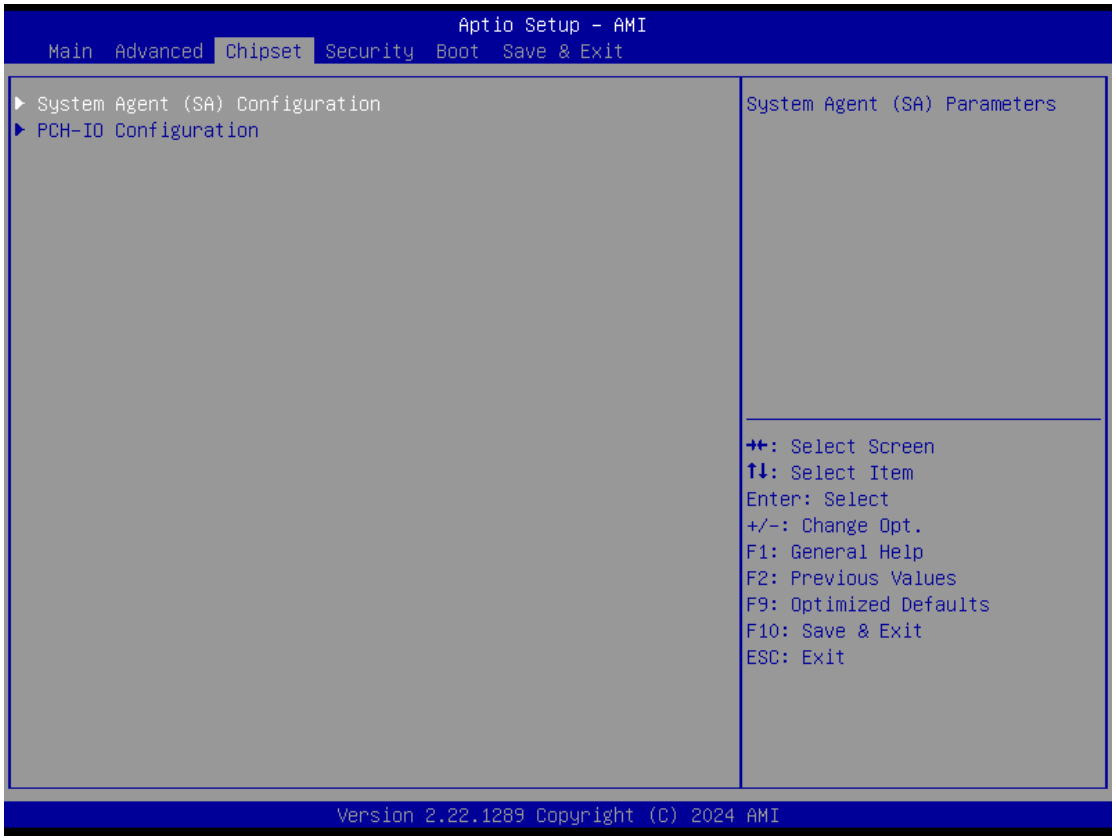
## 3.4.1 PCH-IO Configuration



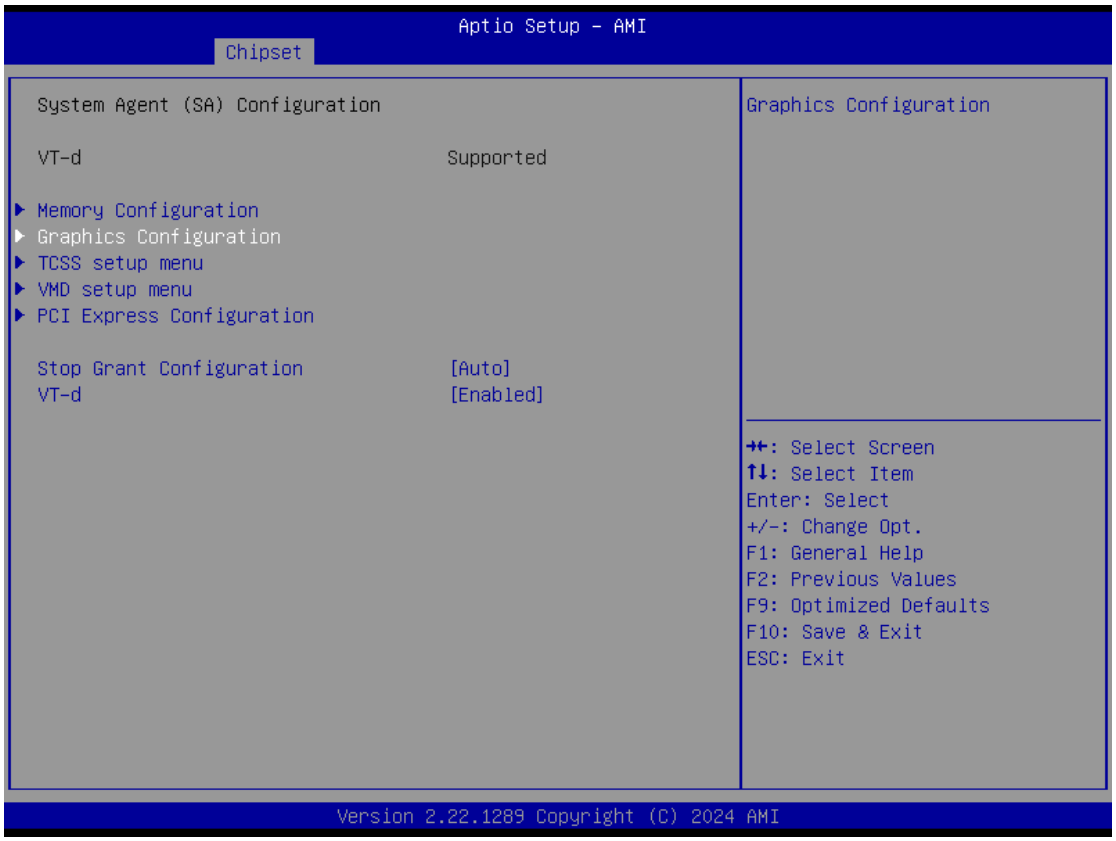

1. **PCI Express Configuration**
2. **SATA Configuration**
3. **USB Configuration**
4. **Security Configuration**
5. **HD Audio Configuration**
6. **State After G3:**
   i. S0 State (system power-on, self-start)
   ii. S5 State (system power-on, shutdown). Set by default.

### 3.4.2 Steps to Configure LVDS in BIOS

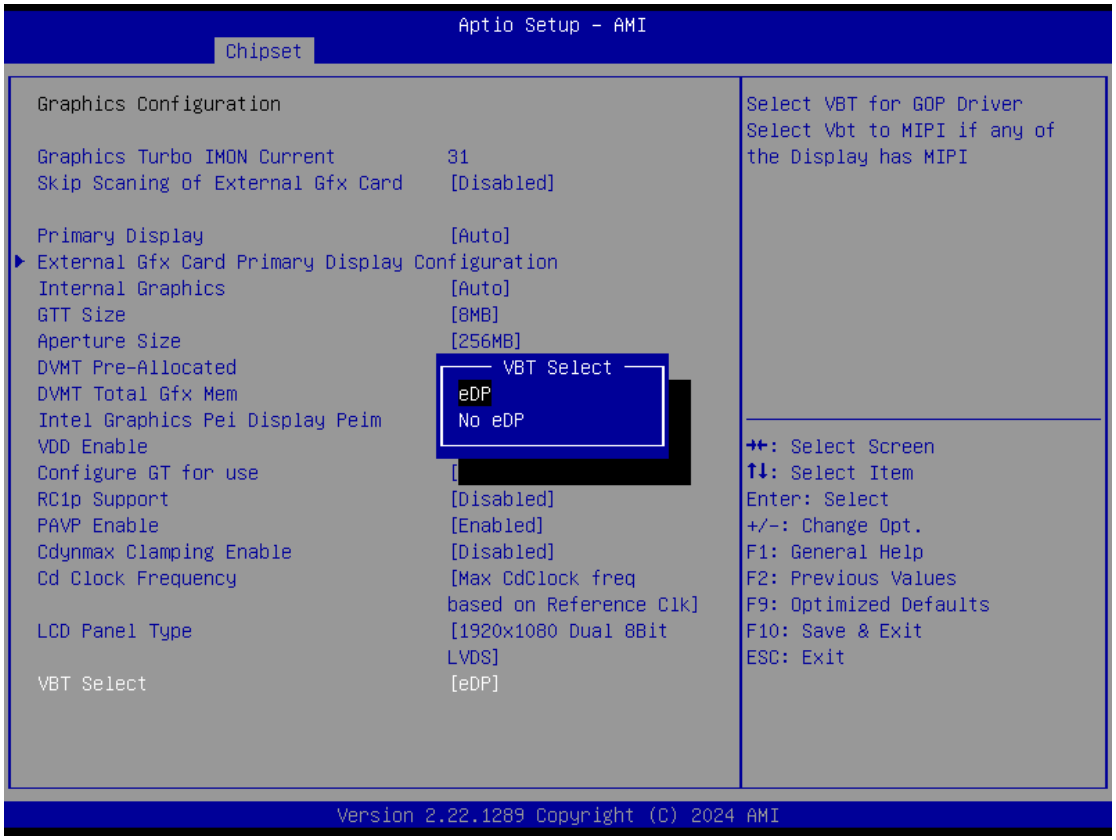
1. Press the DEL key to enter the bios interface, use the left and right arrow keys on the keyboard to get the Chipset section, select "System Agent (SA) Configuration" to enter, as shown below:



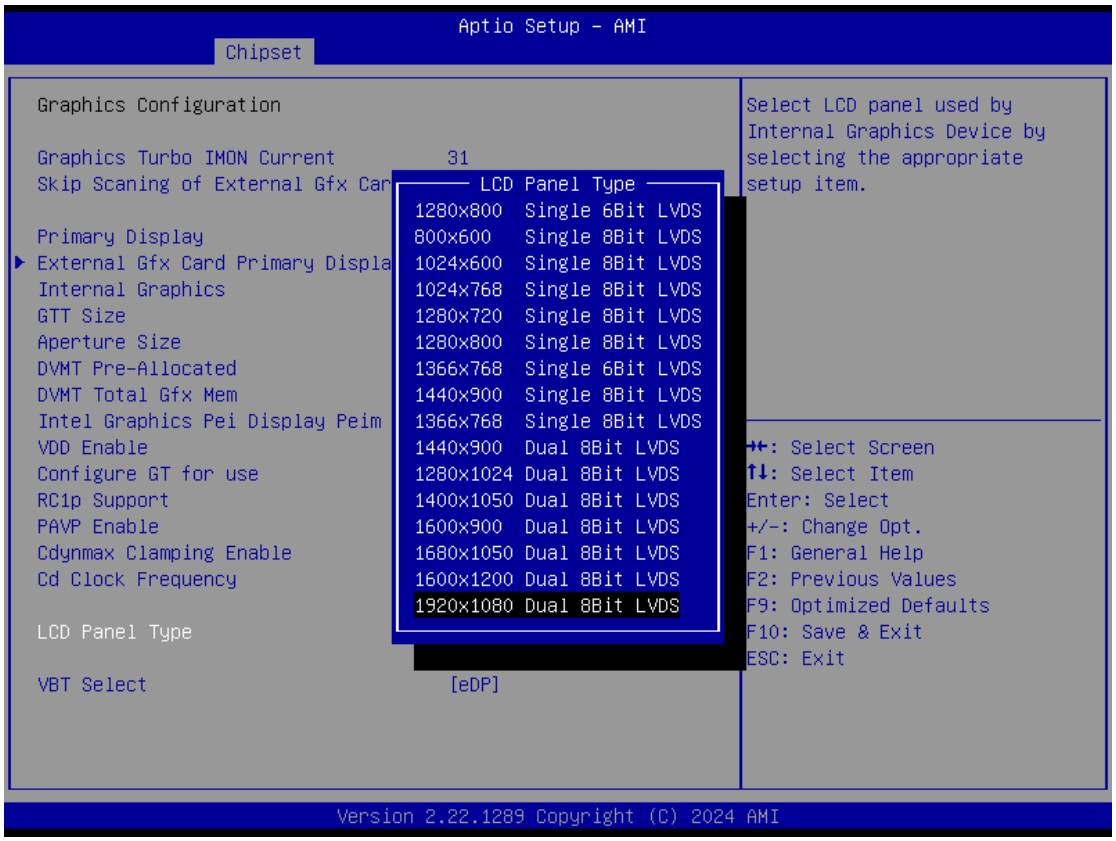
2. Select "Graphics Configuration" then press enter, as shown below:




3. Select the "VBT Select" option to turn the LVDS ON or OFF (LVDS OFF: No eDP, LVDS ON: eDP) as shown below:



4. Select "LCD Pane Type" press enter, then select the target resolution (each monitor's tech specification has the screen-supported resolution), 5After selecting the target screen resolution, press F10 to save and exit. Reference as shown below:



## 3.5 Security

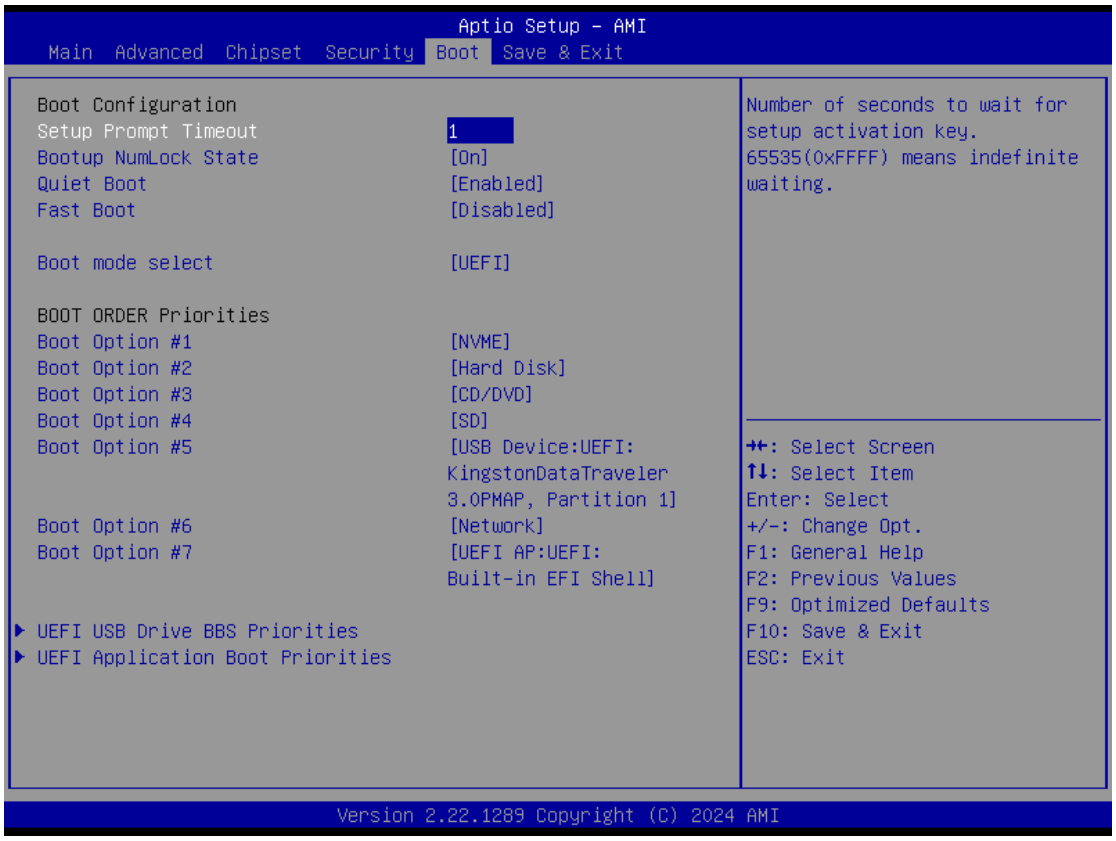



**Administrator Password:** Set the Administrator Password.

**User Password:** Set User Password.

**Secure Boot:** Secure boot

## 3.6 Boot




**Setup Prompt Timeout:**

Number of seconds that the firmware will wait before initiating the original default boot selection. A value of 0 indicates that the default boot selection is to be initiated immediately on boot. A value of 65535(0xFFFF) indicates that firmware will wait for user input before booting. This means the default boot selection is not automatically started by the firmware.

**Bootup NumLock State:**

Select the keyboard NumLock state

**Boot Option #1~#7:**

Set the system boot order from Number 1 to Number 7.

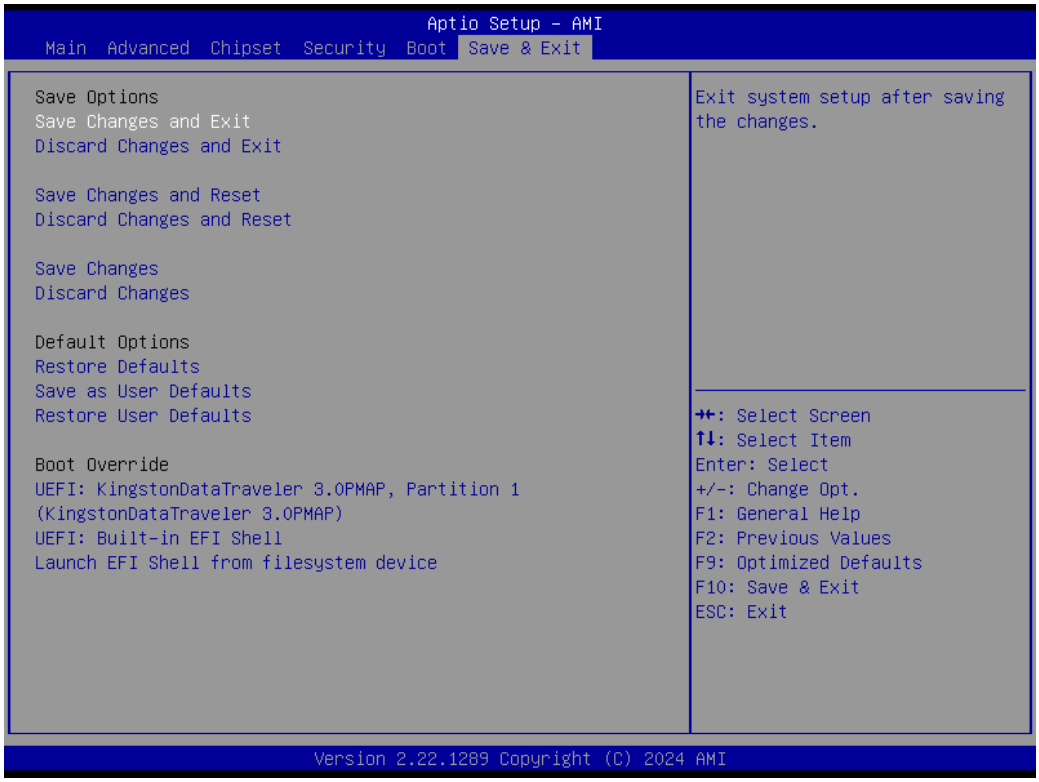
**UEFI USB Drive BBS Priorities**:

UEFI USB Drive BBS priorities setting.

**UEFI Application boot Priorities:**

UEFI application boot priority.

## 3.7 Save & Exit




**Save Changes and Exit:**

Exit the system setup after saving the changes and continue to start the computer.

**Discard Changes and Exit:**

Exit the system setup without saving any changes and continue to start the computer.

**Save Changes and Reset:**

Reset the system after saving the changes.

**Discard changes and Reset:**

Reset the system without saving any changes.

**Save Changes:**

Save changes done so far to any of the options.

**Discard Changes:**

Discard changes done so far to any of the options.

**Restore Defaults:**

Restore/load default values for all the options.

**Save as User Defaults:**

Save the changes done so far as the user defaults.

**Restore User Defaults:**

Restore the user defaults to all the options.

**Boot Override:**

Boot device selection can override your boot priority. Select the specified boot device such as SATA, USB Flash Disk, EFI Shell, PXE, etc., and boot directly. Or press F11 boot by selecting the specified boot device.

Pressing F11 during startup allows you to directly select a specific device to boot from.

# Appendix

## GPIO Setting

Accessing GPIO70:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x01);  //Bit0=1 set as output，bit0=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x01); // When set as output, Bit0 of I/O address 0xA06 = 1 outputs high level, Bit0 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00);  //Bit0=1 Set as output，bit0=0 Set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp =  ReadIo8 (0xA06); //When set as input, Bit0 of I/O address 0xA06 reflects the read state.

Accessing GPIO71:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x02);    // Bit1=1 set as output，bit1=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x02); // When set as output, Bit1 of I/O address 0xA06 = 1 outputs high level, Bit1 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    // Bit0=1 set as output，bit1=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit1 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO72:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x04);  //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x04); // When set as output, Bit2 of I/O address 0xA06 = 1 outputs high level, Bit2 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00);  //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp =  ReadIo8 (0xA06); // When set as input, Bit2 of I/O address 0xA06 reflects the read state.

Accessing GPIO73:

Example: Accessing via IO

Set as output：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x08);  //Bit3=1 set as output，bit3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x08); // When set as output, Bit3 of I/O address 0xA06 = 1 outputs high level, Bit3 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00);  //Bit3=1 set as output，bi3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp =  ReadIo8 (0xA06); // When set as input, Bit3 of I/O address 0xA06 reflects the read state.

Accessing GPIO74:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x10);  //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x10); // When set as output, Bit4 of I/O address 0xA06 = 1 outputs high level, Bit4 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00);  //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp =  ReadIo8 (0xA06); // When set as input, Bit4 of I/O address 0xA06 reflects the read state.

Accessing GPIO75:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x20);  //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x20); // When set as output, Bit5 of I/O address 0xA06 = 1 outputs high level, Bit5 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00);  //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp =  ReadIo8 (0xA06); // When set as input, Bit5 of I/O address 0xA06 reflects the read state.

Accessing GPIO76:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x40);  //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x40); // When set as output, Bit6 of I/O address 0xA06 = 1 outputs high level, Bit6 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00);  //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp =  ReadIo8 (0xA06); // When set as input, Bit6 of I/O address 0xA06 reflects the read state.

Accessing GPIO77:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x80);  //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x80); // When set as output, Bit7 of I/O address 0xA06 = 1 outputs high level, Bit7 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00);  //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp =  ReadIo8 (0xA06); // When set as input, Bit7 of I/O address 0xA06 reflects the read state.