User Manual

MTL-35

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MAXIMIZING YOUR COMPUTING PRODUCTIVITY

MTL-35 User Manual

(Version 0.5)

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V0.5	Initial Version	2026/05/22

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Warning

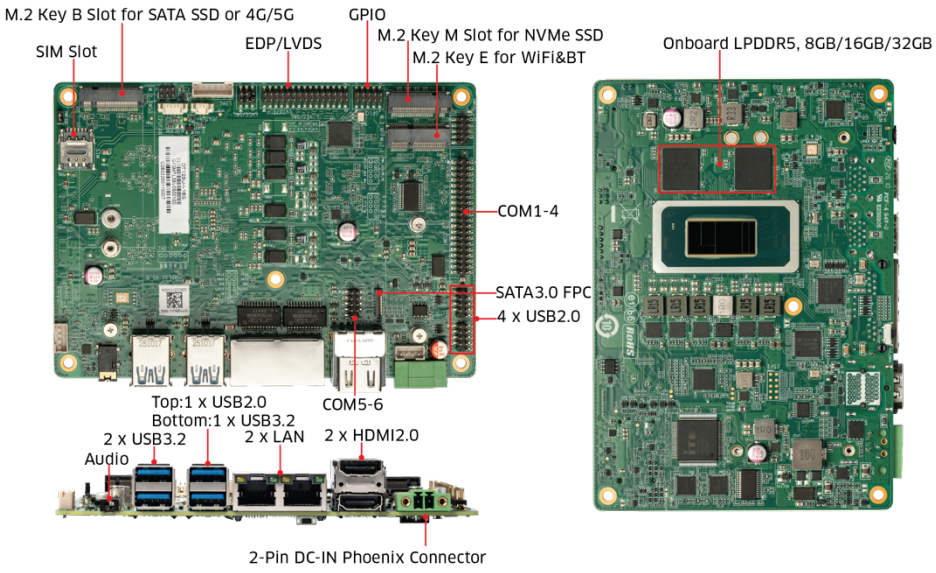
1. Before using the product, carefully read the manual to ensure proper installation and operation.
2. If you are not ready to install any extension card, store it in an anti-static protective bag to prevent damage.
3. To discharge any static electricity, briefly touch a grounded metal object before removing the extension card from the protective bag.
4. Always wear anti-static gloves and handle the card by its edges to avoid damaging sensitive components.
5. Verify that the power supply voltage is correct before connecting the motherboard to the power supply.
6. To prevent electric shock or damage, always turn off the AC power or unplug the power cord before removing or reconfiguring the motherboard or any components.
7. Unplug the AC power cord from the outlet before relocating the motherboard or any components.
8. Ensure all power cords are unplugged before connecting or disconnecting any equipment to avoid electrical hazards.
9. Wait at least 30 seconds after powering off the system before powering it on again to prevent unnecessary wear.
10. If any issues arise during operation, consult a qualified professional for assistance.
11. This product may cause radio interference in certain environments; if necessary, users should take appropriate measures to mitigate such interference.

Contents

Chapter 1 Product Introduction

1.1 Brief Introduction

The MTL35 is a 3.5" single board computer (SBC) based on the Intel® Core™ Ultra Meteor Lake-U/Arrow Lake-U Series platform. It features a compact form factor combined with high performance computing, making it ideal for energy-efficient applications.



1.2 Parameters

CPU: Intel® Core™ Ultra processors/Meteor Lake-U/Arrow Lake-U

CPU	Cores/Threads	Max Turbo Frequency	Base Frequency	Cache	TDP	Overall Peak TOPS (Int8)
125U	12C(2P+8E)/14T	P-Core: 4.3GHz E-Core: 3.6GHz LPE-Core: 2.1GHz	P-Core: 1.3GHz E-Core: 800MHz LPE-Core: 700MHz	12MB	15W Max 57W, Default 15W, PL1/PL2:15W	21
225U	12C(2E+8P)/14T	P-Core: 4.8GHz E-Core: 3.8GHz LPE-Core: 2.4GHz	P-Core: 1.5GHz E-Core: 1.3GHz LPE-Core: 700MHz	12MB	15W Max 57W, Default 15W, PL1/PL2:15W	24

GPU: Integrated Intel Graphics

CPU	GPU Name	Max Dynamic Frequency	GPU Peak TOPS (Int8)	X^e-cores	AI Software Frameworks Supported by GPU
125U	Intel® Graphics	1.85GHz	7	4	OpenVINO™, WindowsML, DirectML, ONNX RT, WebGPU
225U	Intel® Graphics	2.00GHz	8	4	OpenVINO™, WindowsML, DirectML, ONNX RT, WebGPU

NPU:

CPU	NPU Name	NPU Peak TOPS (Int8)	Sparsity Support	Windows Studio Effects Support	AI Software Frameworks Supported by NPU
125U	Intel® AI Boost	11	Yes	Yes	OpenVINO™, WindowsML, DirectML, ONNX RT
225U	Intel® AI Boost	12	Yes	Yes	OpenVINO™, WindowsML, DirectML, ONNX RT

Display Interfaces:

- 2 x HDMI2.0
- 1 x LVDS, eDP optional (labeled as LVDS/EDP on board).

Memory: Onboard LPDDR5-6400MT/s, 8GB/16GB/32GB, support dual channel.

Storage/Expansion:

- 1 x M.2 Key M Slot for 2280 NVMe SSD (labeled as M.2_N on board)
- 1 x M.2 Key B Slot for 2242/2280 SATA SSD or 3042 4G/3052 5G Module (labeled as M.2_SW5G on board)
- 1 x M.2 Key E Slot for 2230 Wi-Fi & BT Module, support PCIE & CNVi/USB2.0 Signal (labeled as M.2_E on board)
- 1 x SATA3.0 FPC Interface (labeled as SATA on board)

Audio: SenaryTech SN6186 High-Definition Audio Codec, support 1 x CTIA Audio Jack, Line_out+Mic_in in one, supports power amplifier.

Ethernet: 2 x Intel i210 Gigabyte Network Controllers, RJ45 interfaces. Date Rate Per Port: 1.0GbEs.

USB:

- 3 × USB 3.2 Gen 2 Type-A rear ports, 10 Gbps (labeled as USB30/USB31 on board).
- 5 × USB 2.0, 480Mbps. 1*shared in rear USB Type-A connector plus 4*onboard header (2.0 mm pitch) (labeled as USB20/USB21 on board)

Serial COM: 6 x COM headers support RS-232 by default. COM1-2 can be optional configurable as RS422/RS485 via BIOS. COM5-6: RS232 (TX/RX/GND only, no flow control)

GPIO: 8-bit GPIO (labeled: GPIO, 2.0 mm)

TPM: External TPM module support (Infineon SLB9670, optional).

Other I/O:

- 1 × JFP Front Panel Header (board label: JFP, 2.0 mm pitch)
- 1 × CN1 Multifunction Header for Hardware Auto Power-On, eDP/LVDS Selection, and External PWR_ON Signal (board label: CN1, 2.0 mm pitch)
- 1 × L_VCC/BKL Header for LCD Panel Voltage Selection and Backlight Polarity Configuration (board label: L_VCC/BKL, 2.0 mm pitch)
- 1 × LBKL LCD Backlight Power Enable Header (board label: LBKL, 2.0 mm pitch)
- 1 × JAUD Audio Amplifier Header (board label: JAUD, 2.0 mm pitch)
- 1 × CPU_FAN 4-pin 5 V CPU Fan Header (board label: CPU_FAN, 1.25 mm pitch)
- 1 × PWR-SSD Voltage Selection Header for the M.2-SW5G SSD/5G Module (2.0 mm pitch)
- 1 × Nano SIM Card Slot

Power:

- 9V-36V via 2-pin DC-IN Phoenix Connector (3.81 mm pitch) by default
- PH4 4-pin power connector (2.0 mm pitch) optional

Operating Temperature: -20℃~60℃

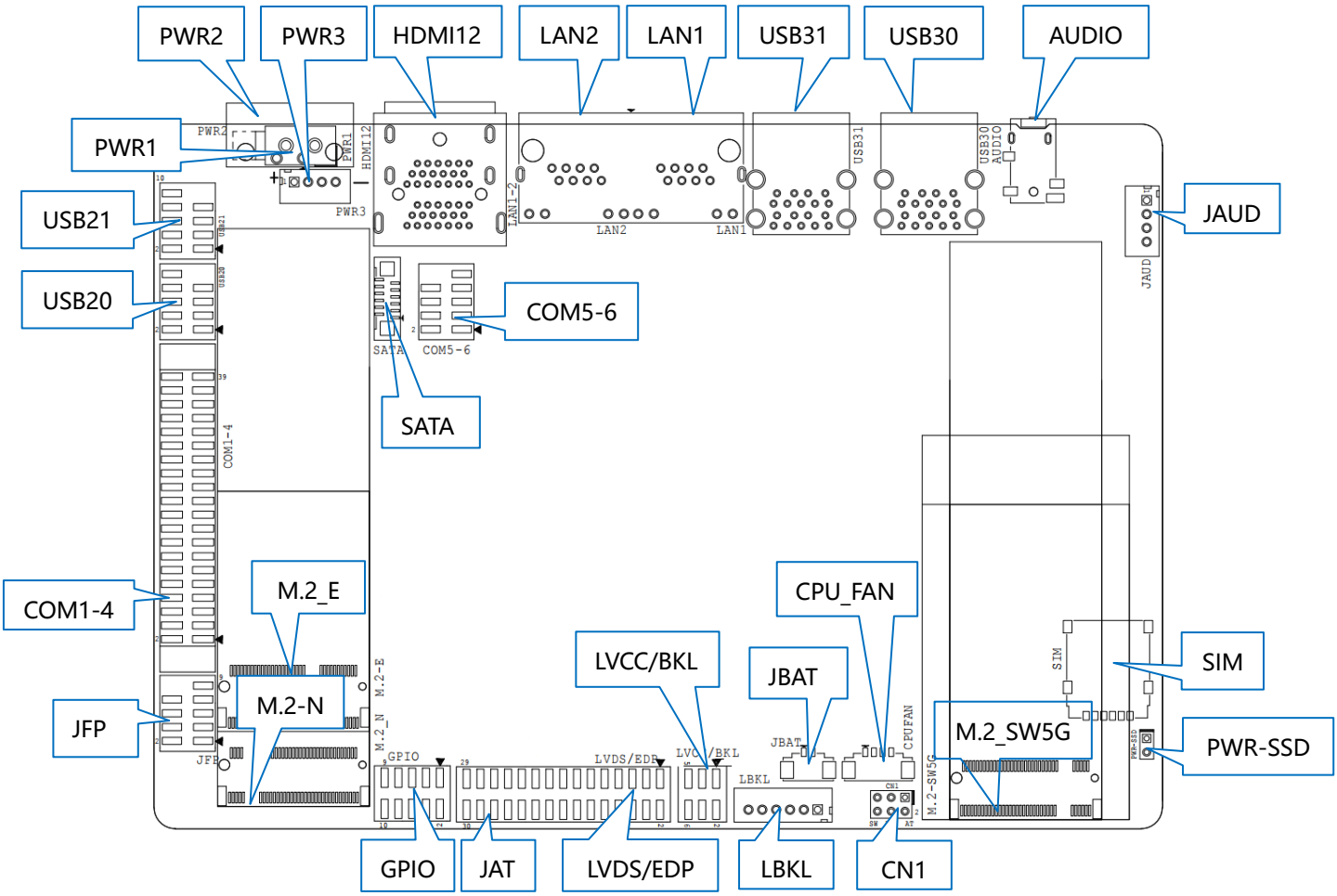
Form Factor: 3.5'' SBC

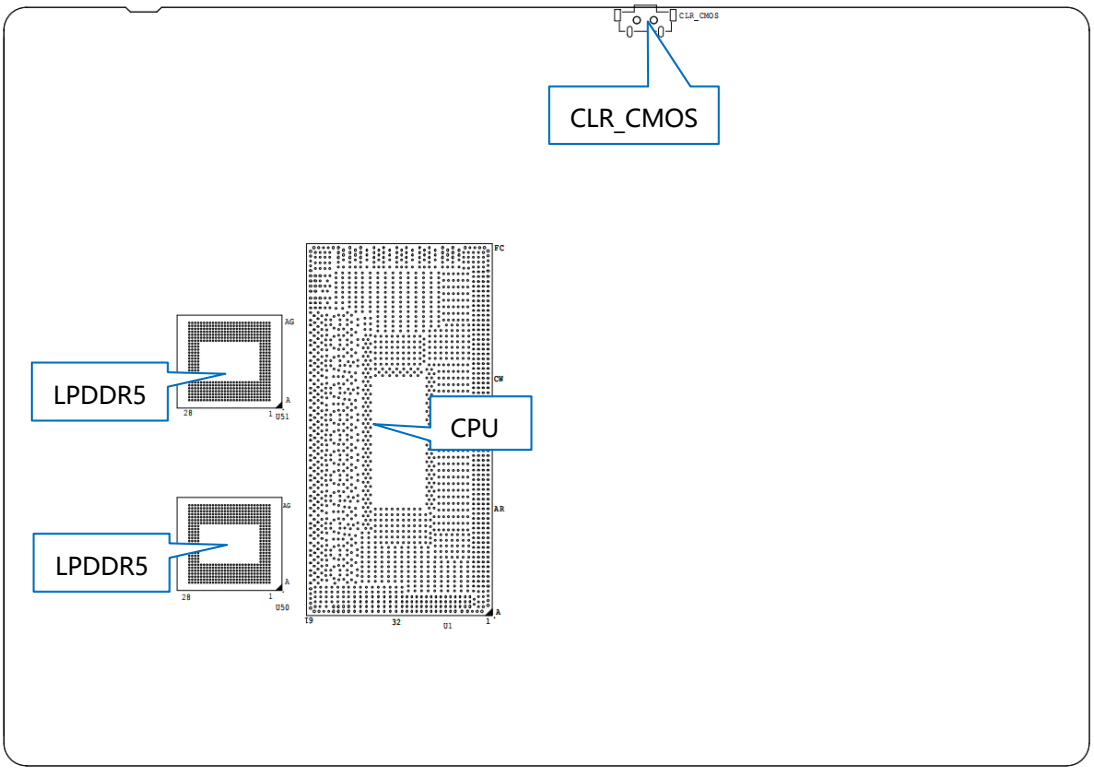
Dimension: 146mm x 102mm

OS Support: Supports Windows® 11 Version 24H2, Ubuntu 24.04 LTS, and later operating systems.

(Note Windows® 10 and operating system versions earlier than Windows® 11 Version 24H2 or Ubuntu 24.04 LTS are not supported. Refer to the official Microsoft and Intel documentation for processor compatibility and operating system support.)

1.3 Connector Diagram





Chapter 2 Hardware

2.1 Installations

Please refer to the following steps for installation:

1. Read the user manual carefully to make sure all the adjustments on the MTL35 are correct.
2. Installing the Memory:
    - Press the ejector tab of the memory slot outwards with your fingertips.
    - Hold the memory module and align the key to the module with that on the memory slot.
    - Gently push the module into the slot until the ejector levers return completely to the closed position, holding the module in place when the module touches the bottom of the slot. To remove the module, press the ejector levers outwards to unseat the module.
3. Installing the expansion cards:
    - Locate the expansion slots and remove the screw, insert the cards into the slot at a 45-degree angle then attach the screw to the expansion cards, gently press down on it then install the screw back.
4. Connect all signal wires, cables, panel control wiring, and power supplies.
5. Start the computer and complete the setup of the BIOS program.

The board's components are integrated circuits and can easily be damaged by Electrostatic Discharge or ESD; therefore, please follow the instructions:

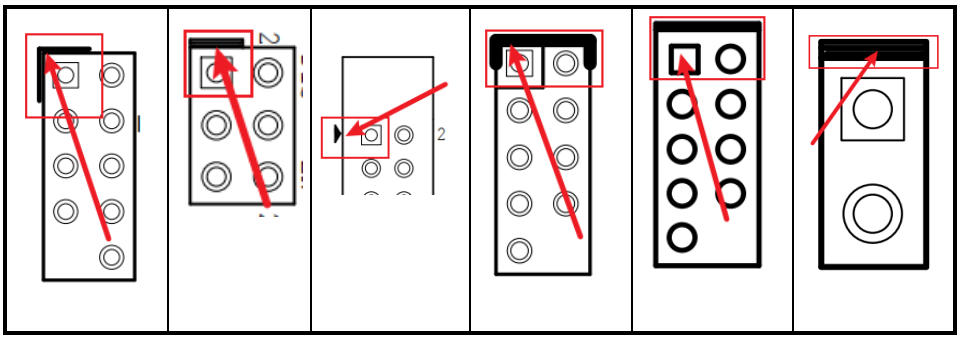
- Hold the board's edge when handing, and do not touch onboard pins, components, or plug sockets.
- When touching integrated circuit components (such as CPU, RAM, etc.), please wear an anti-static wrist strap/glove to avoid electrostatic discharge damage to the board or other sensitive components.
- Before installing the integrated circuits/sensitive components, place the sensitive components in anti-static bags to keep them safe from ESD.
- Please make sure the power switch is OFF before plugging the power plug.

2.2 Jumper Setting

Please configure the jumpers according to your requirements before installing the hardware.

How to identify the first header of jumpers and pins: Observe the mark beside the jumper or pins and find the header marked by “1” or bold line or triangular symbol. Or observe the rear panel and the header with a square solder pad is the first header.

Illustration:

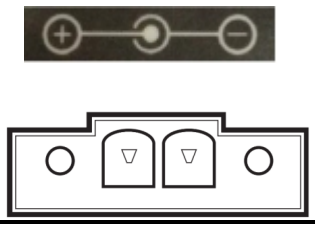
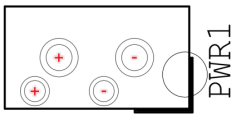
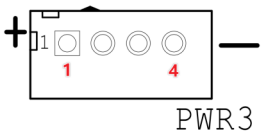


2.3 Memory

The motherboard is equipped with onboard dual-channel LPDDR5 6400MT/s memory, available in 8GB / 16GB / 32GB configurations. The memory is factory-installed and cannot be upgraded.

2.4 Board Power Supply (labeled PWR1, PWR2, PWR3, onboard)

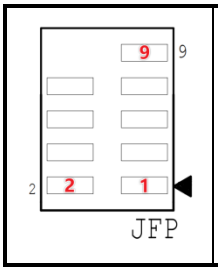
The motherboard supports power input through either a 9–36 VDC 2-pin DC-IN Phoenix connector (3.81 mm pitch) or a PH4 4-pin power connector (2.00 mm pitch).

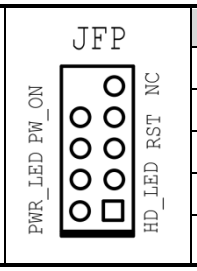
PWR1: DC-IN Phoenix Connector (2PIN) (3.81mm pitch)	**PWR2: Reserved for an optional 2-pin ATX power connector (4.20 mm pitch)**	**PWR3: PH4 4-pin power connector (2.00 mm pitch)**
		

2.5 Front Panel Header (labeled JFP onboard)

The JFP header is used to connect the chassis front panel switches and status LEDs, including the power button, reset button, power LED, and HDD activity LED.

JFP Pin Definition:



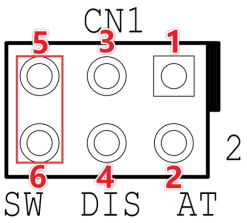


Signal	Pin		Signal
NC	10	9	NC
PWR_ON-	8	7	RSTBTN+
PWR_ON+	6	5	RSTBTN-
PWR_LED-	4	3	HDD_LED-
PWR_LED+	2	1	HDD_LED+

External PWR_ON Header (CN1 Pins 5–6) (labeled CN1 onboard)

The PWR_ON header (Pins 5 and 6) allows connection of an external power button for remote or chassis-mounted power control.

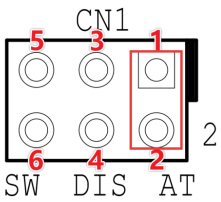
Signal	PWR_ON+	PWR_ON-
Pin	5	6



2.6 Hardware Auto Power-On (labeled CN1 onboard)

The Hardware Auto Power-On function is configured using Pins 1–2 of the CN1 header (labeled CN1 onboard, Pin 1-2). Install a jumper across Pins 1 and 2 to enable automatic power-on when AC power is restored. Remove the jumper to disable the function.

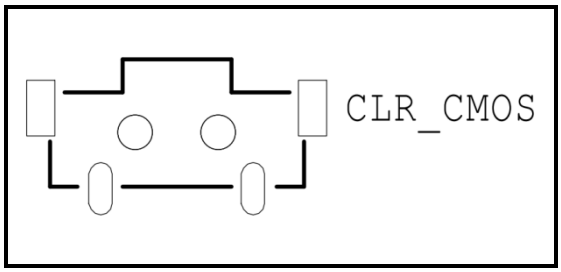
Signal	Enable	Disable
Pin	1-2	NC



2.7 CMOS Clearance/Retention (Labeled CLR_CMOS Onboard)

The CMOS memory is powered by the onboard coin-cell battery. Clearing the CMOS erases all previously saved BIOS settings and restores the BIOS to its factory default configuration.

CMOS Button (Labeled CLR_CMOS onboard)



Steps:

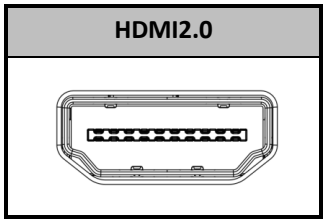
1. Shut down the system and disconnect the power supply.
2. Press and hold the CLR_CMOS button for at least 3 seconds.

⚠ Do not clear the CMOS while the system is powered on, as doing so may damage the motherboard.

2.8 Display Interfaces

The board provides multiple display outputs, including 2x HDMI2.0b, and 1x LVDS (optionally configurable as eDP):

- 2 × HDMI 2.0b port supporting up to 4K @ 30 Hz
- 1 × LVDS header (eDP optional) supporting up to 1920 × 1200, 24-bit.
  When configured as an eDP interface (optional), the header supports 3.3V eDP panels up to 4K @ 30 Hz.



2.8.1 LVDS (Labeled LVDS/EDP, L-BKL, LVCC/BKL, CN1 onboard)

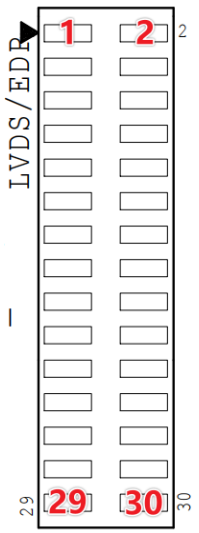
When the interface is configured for LVDS mode, the following headers operate as LVDS-related control and power interfaces:

LVDS/EDP: Carries the LVDS signal lines.

L-BKL: Controls panel backlight on/off and brightness adjustment.

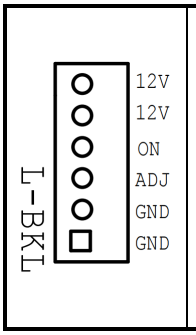
LVCC / BKL: Provides LCD operating voltage selection and backlight polarity (forward/inversion) control.

LVDS Data Pin (labeled EDP/LVDS onboard) (2.0mm):



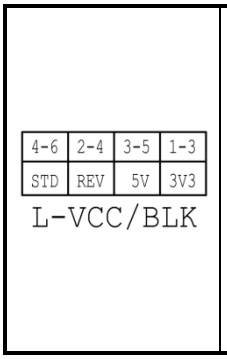
Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	GND
GND	5	6	GND
A_DATA0_DN	7	8	A_DATA0_DP
A_DATA1_DN	9	10	A_DATA1_DP
A_DATA2_DN	11	12	A_DATA2_DP
GND	13	14	GND
A_CLK_DN	15	16	A_CLK_DP
A_DATA3_DN	17	18	A_DATA3_DP
B_DATA0_DN	19	20	B_DATA0_DP
B_DATA1_DN	21	22	B_DATA1_DP
B_DATA2_DN	23	24	B_DATA2_DP
GND	25	26	GND
B_CLK_DN	27	28	B_CLK_DP
B_DATA3_DN	29	30	B_DATA3_DP

LVDS Backlight Connector Pin (Labeled L-BKL onboard):



Pin	Signal
6	12V
5	12V
4	LCD_BKL_ON
3	LCD_BKL_ADJ
2	GND
1	GND

LVDS Operating Voltage and Backlight Polarity Adjustment Pin (Labeled LVCC/BKL onboard):

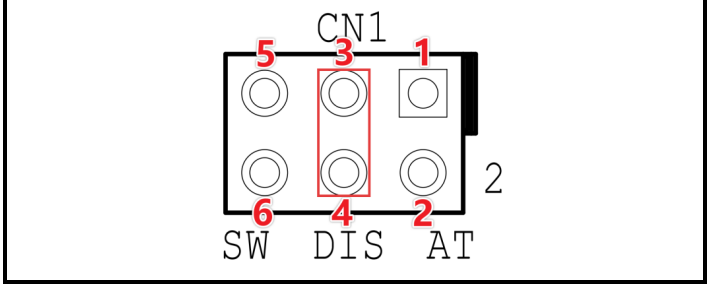


Pin	Setting	Function
1-3	Close	VCC(+3.3V)
3-5	Close	VCC(+5V)
2-4	Close	REV (Backlight Control Reverse)
4-6	Close	STD (Backlight Control Standard)

LVDS Signal Enable/Disable (labeled CN1 onboard, Pin3-4)

The LVDS signal is configured using Pins 3–4 of the CN1 header. Install a jumper across Pins 3–4 to disable the LVDS signal. Remove the jumper to enable the LVDS signal.

Function	Disable LVDS Signal	Enable LVDS Signal
Pin	3-4	NC

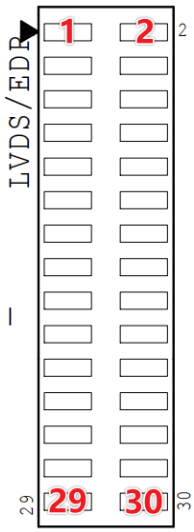


Please Note: *The LVDS operating voltage adjustment switch is pin controlled. By shorting the jumper caps, the voltage can be flexibly adjusted between 3.3V/5V. Based on your LVDS display's voltage parameters, use the jumper caps to short the pins corresponding to the required voltage. (Do not short pins of different voltages simultaneously.)*

2.8.2 eDP (optional)

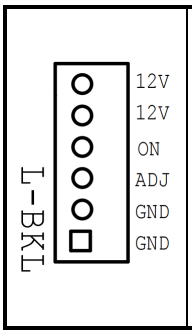
When set to eDP mode, the “EDP/LVDS” pins output eDP signals. The “L-BKL” pins are used for backlight control, and the “LVCC/BKL” pins provide power to the panel and backlight (with forward/inversion adjustment).

eDP Pin Definition (labeled EDP/LVDS onboard) (2.0mm):



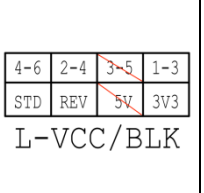
Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	EDP_HPD
GND	5	6	GND
EDP_AUXN	7	8	EDP_AUXP
N/A	9	10	N/A
EDP_DATA0_P	11	12	EDP_DATA0_N
GND	13	14	GND
N/A	15	16	N/A
EDP_DATA1_P	17	18	EDP_DATA1_N
N/A	19	20	N/A
N/A	21	22	N/A
N/A	23	24	N/A
GND	25	26	GND
N/A	27	28	N/A
N/A	29	30	N/A

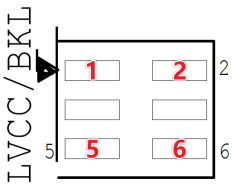
eDP Backlight Brightness Adjustment Pin (labeled L-BKL onboard):



Pin	Signal
6	12V
5	12V
4	LCD_BKL_ON
3	LCD_BKL_ADJ
2	GND
1	GND

eDP Operating Voltage and Backlight Polarity Adjustment Pin (Labeled LVCC/BKL onboard):





Pin	Setting	Function
1-3	Close	VCC(+3.3V)
~~3-5~~	~~Close~~	~~VCC(+5V)~~
~~2-4~~	~~Close~~	~~REV (Backlight Control Reverse)~~
4-6	Close	STD (Backlight Control Standard)

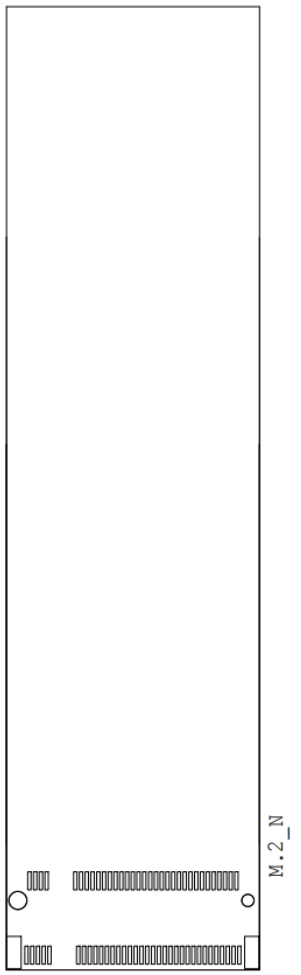
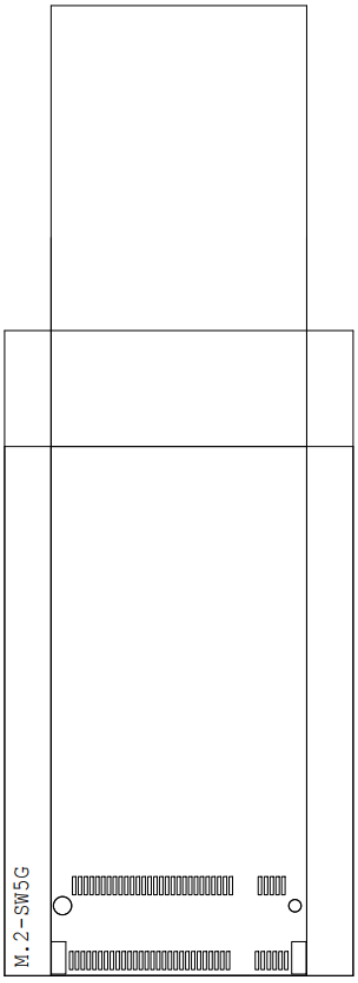
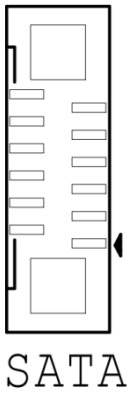
*Note: The eDP panel voltage is configured using jumper settings. eDP panels support **3.3V only**. Install a jumper cap on pins **1–3** to select **3.3V**. **Do not short multiple voltage settings simultaneously**, as this may damage the motherboard or display panel.*

*Entries shown with strike-through indicate functions or settings that are **unavailable or unsupported** in the current configuration and must not be used or configured.*

2.9 Storage Interface (Labeled M.2_N, M.2_SW5G, SATA)

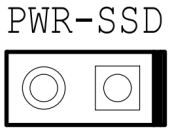
The motherboard provides multiple storage interfaces, including 2 x M.2, 1 x SATA.

- **M.2_N:** 1 x M.2 Key M Slot supporting 2280 NVMe SSDs.
- **M.2_SW5G:** 1 x M.2 Key B Slot supporting 2242/2280 SATA SSD or 3042 4G/3052 5G module.
- **SATA:** FPC SATA connector. An FPC SATA cable is required, with the M-end connected to the onboard SATA connector and the B-end connected to the SATA daughterboard.

M.2_N	M.2-SW5G	SATA
		

The PWR-SSD header is used to configure the operating voltage for the M.2_SW5G slot.

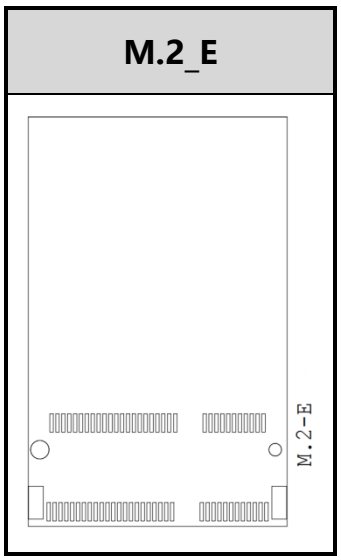
PWR-SSD:

Mode	SSD/4G Module	5G Module
Pin	1-2	NC
		

Note: When installing an M.2 Key B 2242/2280 SATA SSD in the M.2_SW5G slot, install a jumper on the PWR-SSD header (Pins 1–2) to select the SSD/4G Module mode. Failure to configure the PWR-SSD header correctly may result in damage to the installed SSD or 4G/5G module.

2.10 Expansion Slots (Labeled M.2_E onboard)

The motherboard provides 1 x M.2 Key E slot, supporting 2230 Wi-Fi & Bluetooth modules (PCIE& CNVi/USB2.0); labeled M.2_E onboard.

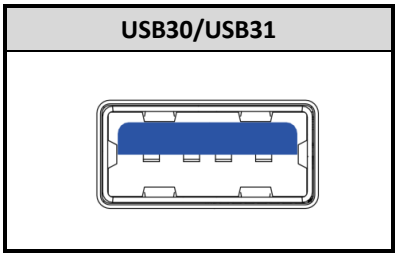


2.11 USB Interfaces (labeled as USB30, USB31, USB20, USB21)

The motherboard supports a total of eight USB interfaces, including 3 x USB 3.2 Gen 2 Type-A ports and 5 x USB 2.0 Type-A ports (4*onboard header+1*shared in rear USB Type-A connector).

USB 3.2

3 x USB 3.2 Gen 2 Type-A rear ports (labeled USB30/USB31 onboard), supporting data transfer rates of up to 10 Gbps.



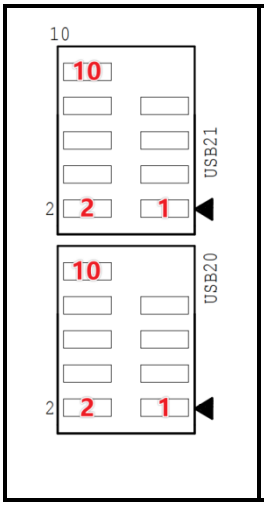
All USB 3.2 Gen 2 ports support 5V Standby (5VSB) power, enabling system wake-up using a USB keyboard or mouse when the system is shut down (with power connected) or in sleep mode. Each port also provides up to 5 V / 1 A power output for external USB devices.

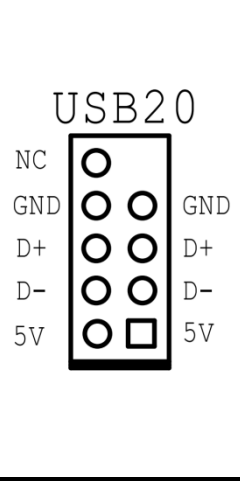
USB 2.0

Two onboard USB 2.0 headers (labeled USB20 and USB21 onboard), supporting up to 4 x USB 2.0 ports with data transfer rates of up to 480 Mbps, plus 1*shared in rear USB Type-A connector.

The USB 2.0 headers provide 5V System (5VS) power and support connection to external USB Type-A ports using a compatible cable or expansion module.

USB Header Pin Definition (labeled as USB20/ USB21):



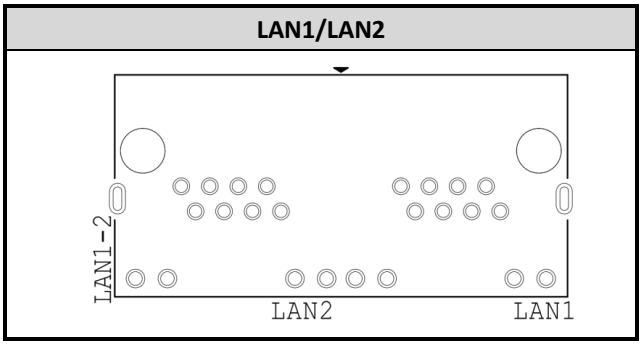


Signal	Pin		Signal
NC	10	9	
GND	8	7	GND
USB DATA+	6	5	USB DATA+
USB DATA-	4	3	USB DATA-
VCC 5V	2	1	VCC 5V

2.12 LAN (labeled as LAN1/LAN2)

The board provides two Gigabit Ethernet RJ45 ports powered by Intel i210 controllers. Both ports support Wake-on-LAN (WoL) via Magic Packet, while LAN1 additionally supports PXE boot.

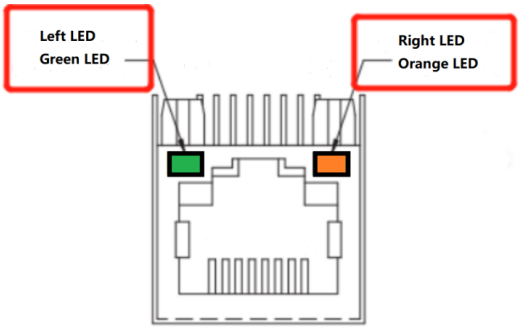
LAN1/LAN2



*Note: Due to Intel® Meteor Lake and Arrow Lake-U platform limitations, Wake-on-LAN (Magic Packet) from the S0 power state is **not supported**.*

LAN Port LED Status Indicators:

LI_LED (Green)	Function	ACT_LED (Orange)	Function
On	Link Established	Blinking	Network Activity



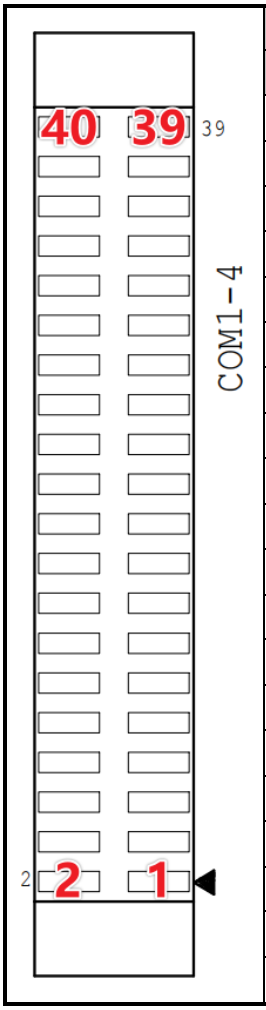
2.13 Serial Ports (Labeled as COM14, COM56)

The motherboard provides six serial ports through two onboard 2.00 mm pitch headers. COM1–COM4 are routed to the COM14 header, while COM5–COM6 are routed to the COM56 header. By default, all serial ports operate in RS-232 mode.

- **COM1/COM2:** RS-232 (default); configurable to RS-422 or RS-485 in the BIOS.
- **COM3/COM4:** RS-232 only.
- **COM5/COM6:** RS-232 only; supports TX, RX, and GND signals only.

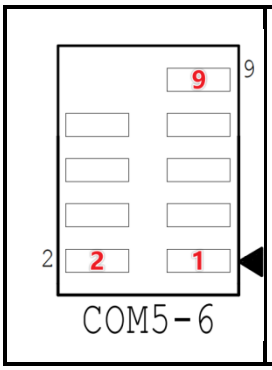
COM1–COM4 provide powered serial interfaces. When the system is powered by 12 VDC, the output voltage follows the input supply voltage (typically 9–13.5 VDC, up to 13 VDC maximum).

COM1_4 Pin Definition (Labeled as COM14)



RS232				COM1/2 Pin Definitions in RS485 mode				COM1/2 Pin Definitions in RS-422			
Signal	Pin		Signal	Signal	Pin		Signal	Signal	Pin		Signal
VCC	40	39	RI#								
CTS#	38	37	RTS#								
DSR#	36	35	GND								
DTR#	34	33	TXD								
RXD	32	31	DCD#								
VCC	30	29	RI#								
CTS#	28	27	RTS#								
DSR#	26	25	GND								
DTR#	24	23	TXD								
RXD	22	21	DCD#								
VCC	20	19	RI#	VCC	20	19	NC	VCC	20	19	NC
CTS#	18	17	RTS#	NC	18	17	NC	NC	18	17	NC
DSR#	16	15	GND	NC	16	15	GND	NC	16	15	GND
DTR#	14	13	TXD	NC	14	13	NC	RX-	14	13	RX+
RXD	12	11	DCD#	DATA+	12	11	DATA-	TX+	12	11	TX-
VCC	10	9	RI#	VCC	10	9	NC	VCC	10	9	NC
CTS#	8	7	RTS#	NC	8	7	NC	NC	8	7	NC
DSR#	6	5	GND	NC	6	5	GND	NC	6	5	GND
DTR#	4	3	TXD	NC	4	3	NC	RX-	4	3	RX+
RXD	2	1	DCD#	DATA+	2	1	DATA-	TX+	2	1	TX-

COM5_6 Pin Definition (Labeled as COM56)

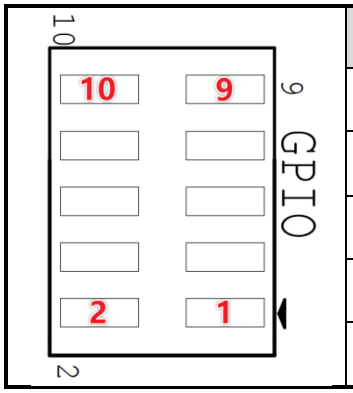


Signal	Pin		Signal
NC	10	9	NC
TX6	8	7	TX5
GND	6	5	GND
RX6	4	3	RX5
NC	2	1	NC

2.14 GPIO (Labeled GPIO onboard)

The motherboard provides a 2×5-pin JGPIO header (Labeled GPIO onboard, 2.0 mm pitch), providing eight programmable GPIO ports. Please refer to the appendix for GPIO configuration details.

GPIO:



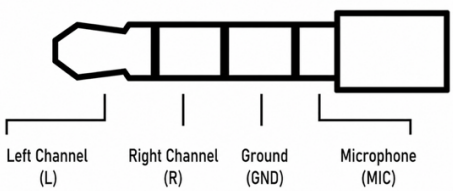
Signal	Pin		Signal
SIO_GP77	10	9	GND
SIO_GP76	8	7	SIO_GP73
SIO_GP75	6	5	SIO_GP72
SIO_GP74	4	3	SIO_GP71
3.3V	2	1	SIO_GP70

2.15 Audio (labeled AUDIO, JAUD onboard)

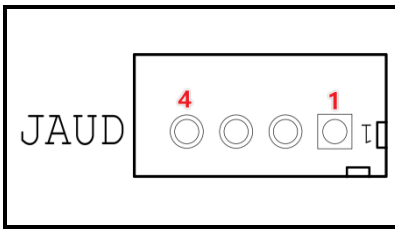
The motherboard integrates the SenaryTech SN6186 High-Definition Audio codec and supports one 3.5 mm CTIA combo audio jack (Line-out + Mic-in), labeled AUDIO on board.

In addition, the board provides a built-in dual-channel amplifier output for connecting passive speakers. The amplifier output is available through the JAUD (labeled JAUD on board) header (2.0 mm pitch).

CTIA combo audio jack (Line-out + Mic-in in one):



JAUD Amplifier Output Header (Labeled JAUD onboard, 2.0mm):



Pin	Signal
1	L+
2	L-
3	R-
4	R+

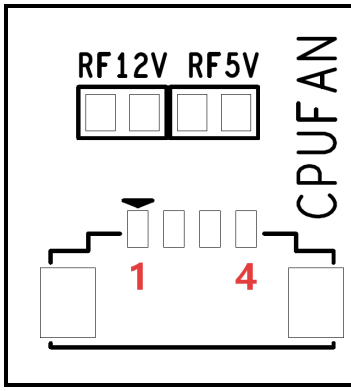
External Speaker Output Specifications (VDD = 5V)

Condition	Output Power
THD=1%, ClassD f=1KHz, RL =4Ω	2.1 W
THD=10%, ClassD f=1KHz, RL =4Ω	3.0 W
THD=1%, ClassD f=1KHz, RL =8Ω	1.4 W
THD=10%, ClassD f=1KHz, RL =8Ω	1.7 W

2.16 CPU Fan/System Fan Socket (Labeled as CPU-FAN)

The motherboard provides one 5 V, 4-pin fan header (1.25 mm pitch), labeled CPU-FAN on the motherboard.

CPU Fan Definition (Labeled CPU-FAN onboard):

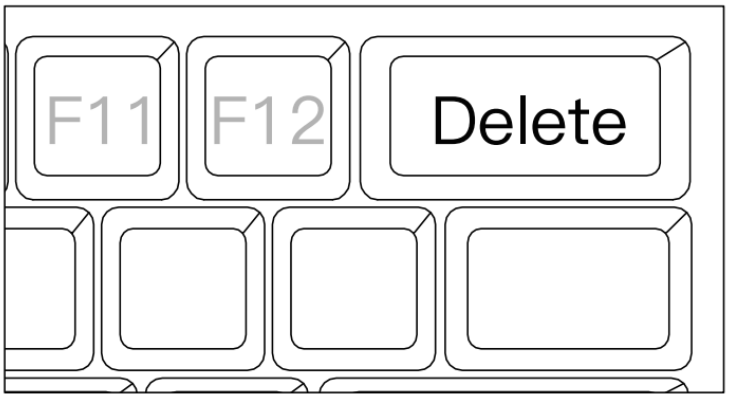


Pin	1	2	3	4
Signal	5V	GND	TAC	CTL
Default Configuration (Resistors RF5V populated)	5V			
Optional Configuration (Resistors RF12V populated)	12V			

Chapter 3 BIOS Setup

3.1 Entering the BIOS

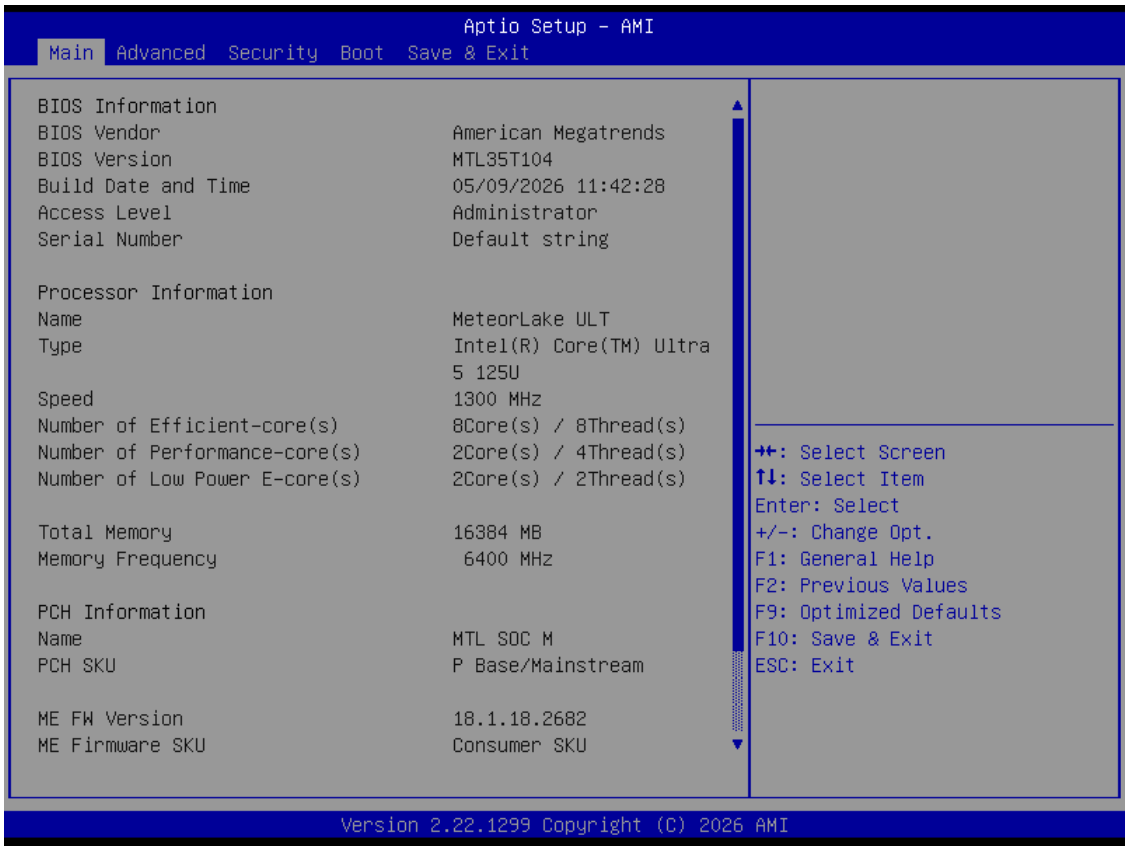
Entering BIOS Setup: Press the <Delete> key repeatedly during system startup to enter the BIOS Setup Utility.



BIOS Hot Keys:

Key	Function	Description
→ ←	Select Screen	Navigate between menu screens.
↑ ↓	Select Item	Move between menu items or options.
Enter	Select	Open a submenu or confirm a selection.
+/-	Change Option	Adjust values or change settings.
F1	General Help	Displays helpful information for the selected item.
F2	Previous Values	Load the previously saved settings.
F9	Optimized Defaults	Restore factory default settings.
F10	Save & Exit	Save changes and exit BIOS.
ESC	Exit	Exit BIOS or return to the previous menu.

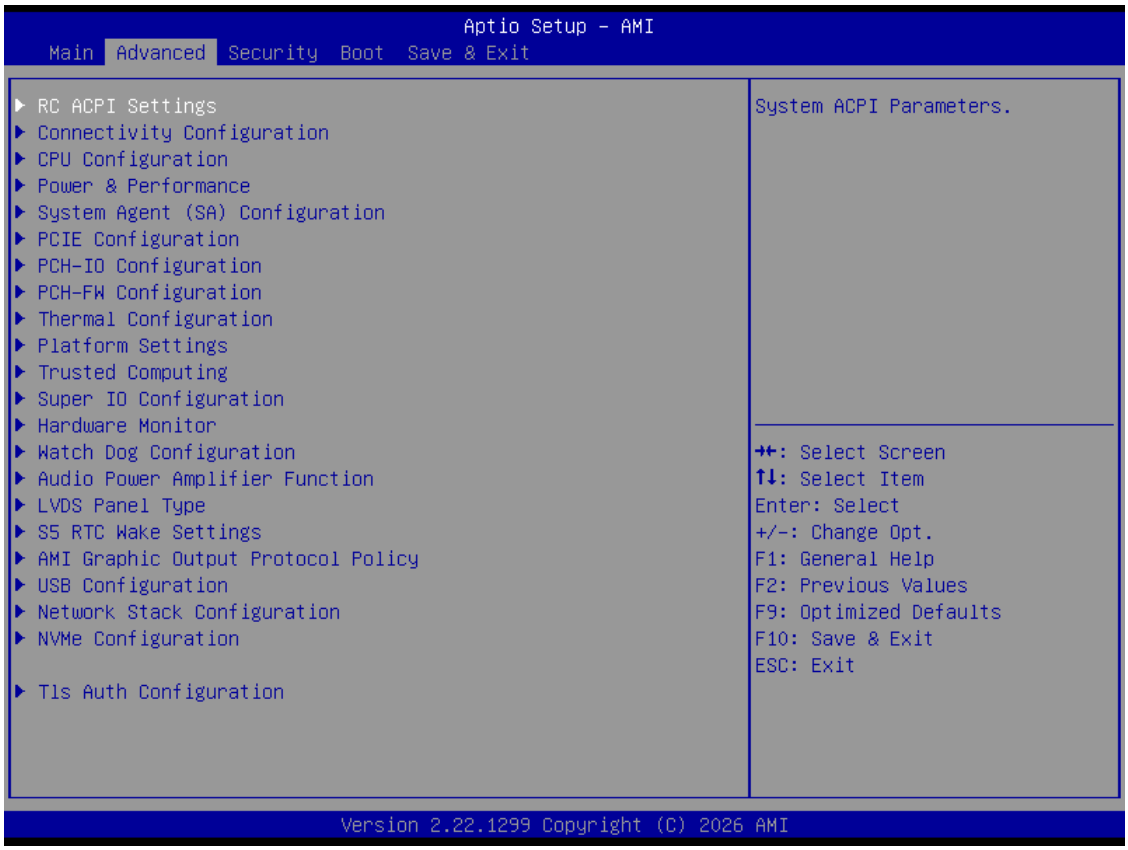
3.2 Main Menu (BIOS Info, Date, Time)



BIOS Information

- BIOS Vendor: American Megatrends
- BIOS Version: Displays the current BIOS version
- Build Date and Time: BIOS build timestamp
- Processor Information: CPU identification details
- Total Memory: Installed system memory
- Memory Frequency: Active memory operating frequency
- PCH Information: Platform Controller Hub details
- PCH SKU: PCH model identifier
- ME FW Version: Intel Management Engine firmware version
- System Date: System date setting (format: MM/DD/YYYY)
- System Time: System time setting (format: HH:MM:SS)

3.3 Advanced Settings



The Advanced menu provides access to the following configuration options:

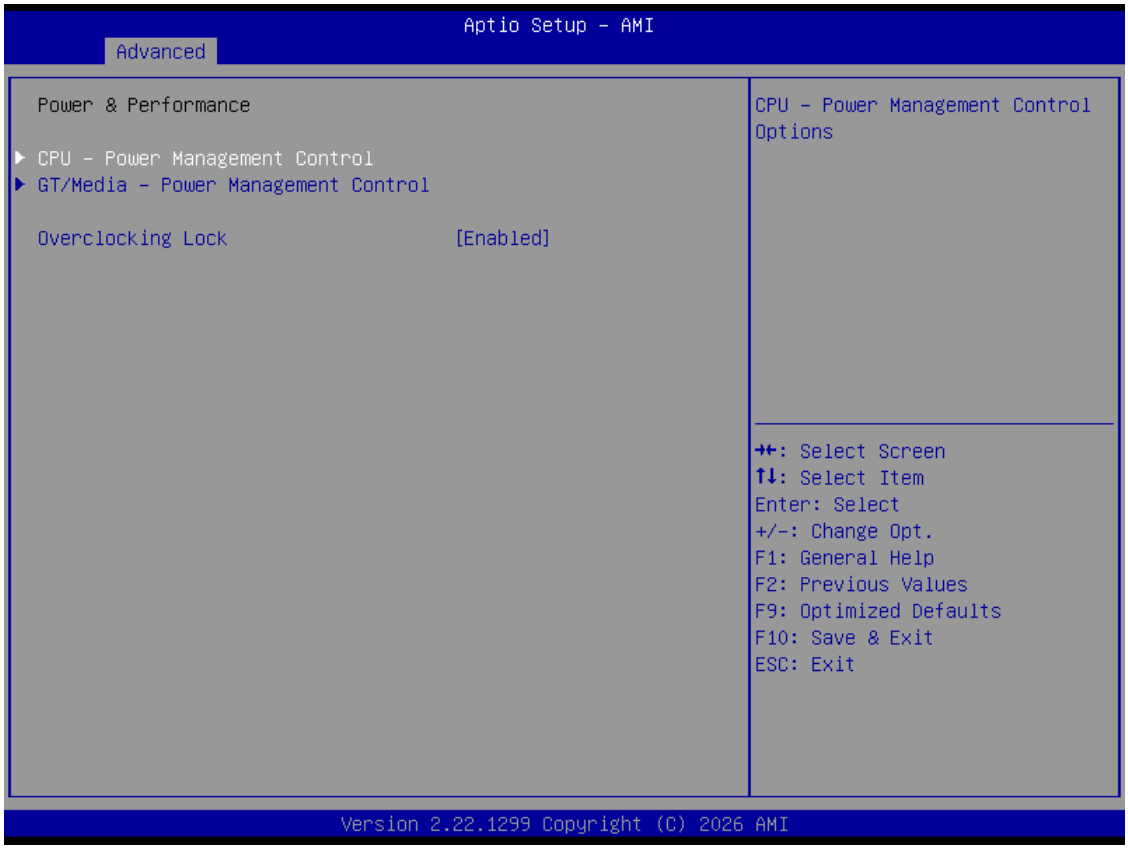
PCH-FW Configuration

- **RC ACPI Settings** – Configures ACPI power management settings.
- **Connectivity Configuration** – Configures onboard connectivity features and interfaces.
- **CPU Configuration** – Configures processor features and CPU-related settings.
- **Power & Performance** – Configures CPU power management and performance settings.
- **System Agent (SA) Configuration** – Configures graphics memory allocation, display options, and other System Agent settings.
- **PCIe Configuration** – Configures PCI Express devices and link settings.
- **PCH-IO Configuration** – Configures Platform Controller Hub (PCH) I/O functions and onboard peripherals.
- **PCH-FW Configuration** – Configures Platform Controller Hub (PCH) firmware settings.
- **Thermal Configuration** – Configures thermal management and temperature control settings.
- **Platform Settings** – Configures platform-specific hardware settings.
- **Trusted Computing** – Configures TPM and trusted computing features.
- **Super IO Configuration** – Configures Super I/O controller settings.
- **Hardware Monitor** – Displays system voltage, temperature, fan speed, and hardware status.
- **Watch Dog Configuration** – Configures the watchdog timer.
- **Audio Power Amplifier Function** – Configures the onboard audio power amplifier.
- **LVDS Panel Type** – Configures LVDS panel parameters and display settings.
- **S5 RTC Wake Settings** – Configures RTC-based automatic power-on from the S5 (Soft Off)

state.

- **AMI Graphic Output Protocol Policy** – Configures AMI Graphics Output Protocol (GOP) settings.
- **USB Configuration** – Configures USB controller and device settings.
- **Network Stack Configuration** – Configures the UEFI network stack and PXE boot settings.
- **NVMe Configuration** – Displays information for installed NVMe devices.
- **Tls Auth Configuration** – Configures TLS authentication settings

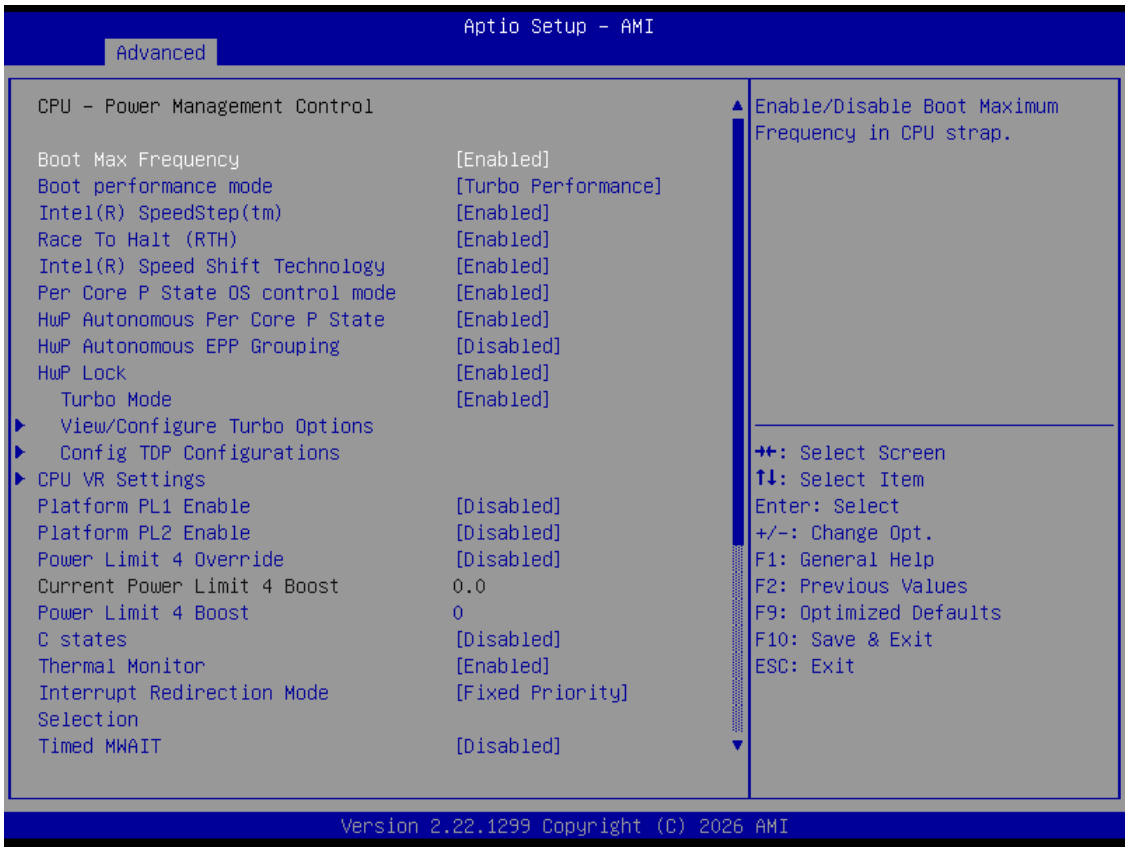
3.3.1 Power & Performance



The Power & Performance menu provides configuration options for processor power management, graphics power management, and overclocking control.

- **CPU Power Management Control** – Configures processor power management features, power-saving technologies, and CPU operating states.
- **GT / Media Power Management Control** – Configures power management settings for the integrated graphics (GT) and media engine.
- **Overclocking Lock** – Enables or disables overclocking configuration to prevent unauthorized modification of processor performance settings.

3.3.2 CPU-Power Management Control

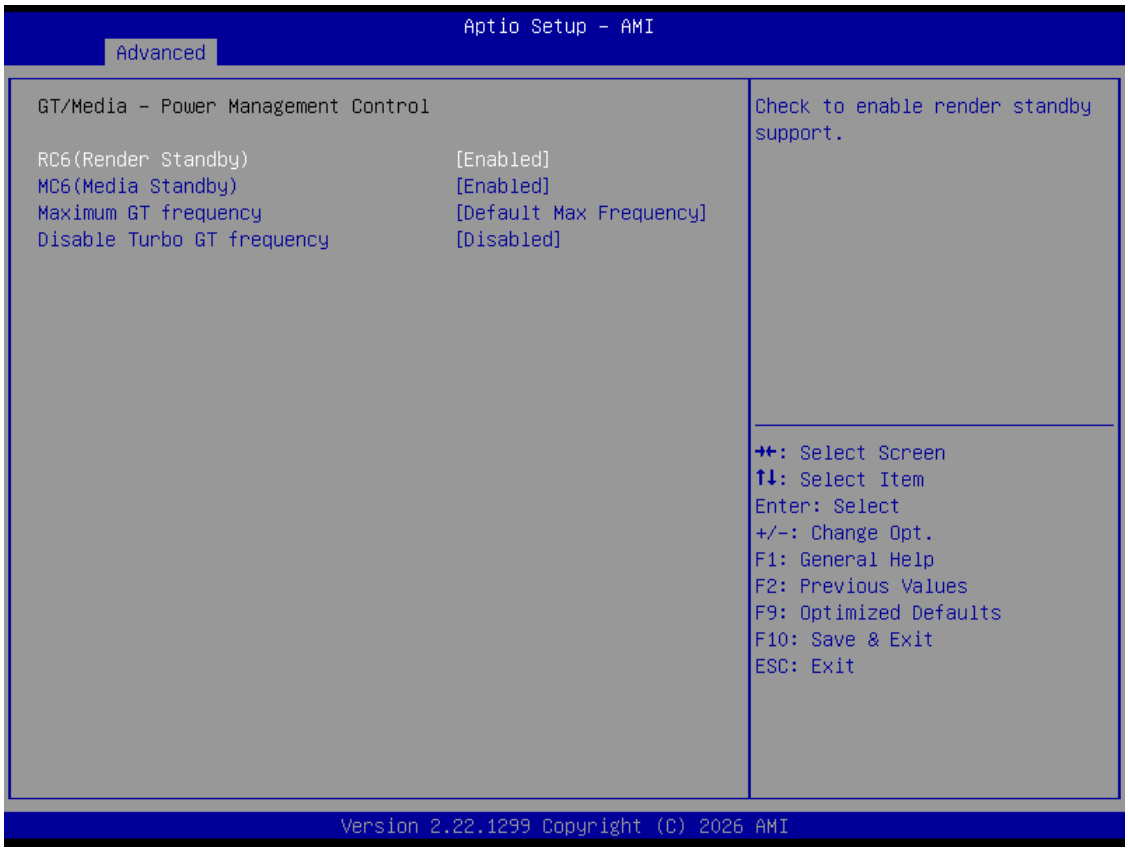


The CPU Power Management Control menu provides configuration options for processor power management, performance optimization, and power-saving features.

- **Boot Max Frequency** – Enables or disables booting the processor at its maximum operating frequency. Default: Enabled.
- **Boot Performance Mode** – Selects the processor performance profile during system boot. Available options include Turbo Performance (default), Max Battery, and Max Non-Turbo Performance.
- **Intel® SpeedStep® Technology** – Enables or disables Intel® Enhanced SpeedStep® Technology, allowing the processor to dynamically adjust its operating frequency and voltage based on system workload. Default: Enabled.
- **Intel® Speed Shift Technology** – Enables or disables Intel® Speed Shift Technology, allowing the processor to autonomously manage frequency and voltage transitions for improved performance responsiveness and power efficiency. Default: Enabled.
- **Per Core P-State OS Control Mode** – Enables operating system control of processor performance states (P-states) on a per-core basis.
- **HWP Autonomous Per Core P-State** – Enables autonomous Hardware P-state (HWP) management for individual processor cores.
- **HWP Autonomous EPP Grouping** – Configures Hardware P-state (HWP) Energy Performance Preference (EPP) grouping behavior.
- **EPB Override over PCIe –** Configures Energy Performance Bias (EPB) override for PCIe devices.
- **Platform PL1 Enable –** Enables or disables Platform Power Limit 1 (PL1). Default: Disabled.
- **Platform PL2 Enable** – Enables or disables Platform Power Limit 2 (PL2). Default: Disabled.

- **Power Limit 4 Override** – Enables or disables Power Limit 4 (PL4) override. Default: Disabled.
- **C-States –** Enables or disables processor idle power states to reduce power consumption during periods of low CPU utilization. Default: Enabled.
- **Enhanced C-States –** Enables enhanced processor idle power states for additional power savings during idle operation. Default: Enabled.

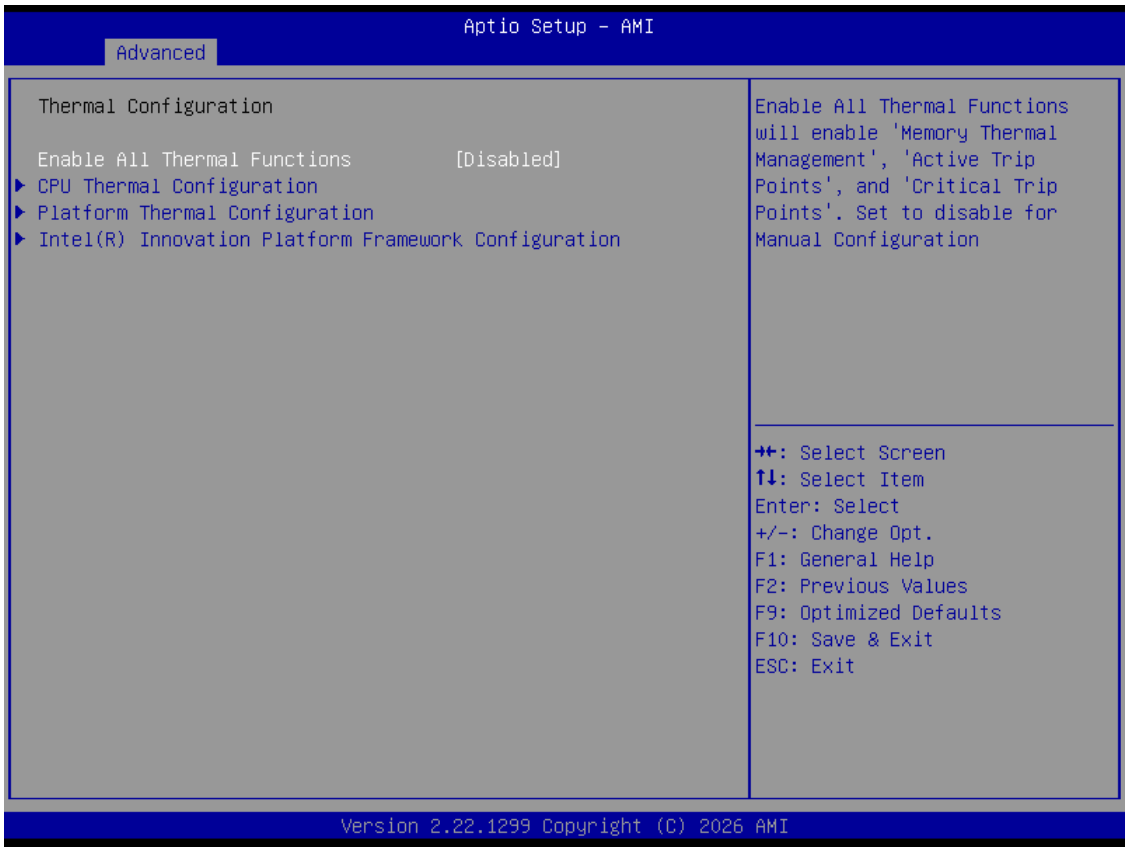
3.3.3 GT/Media-Power Management Control



The GT / Media Power Management Control menu provides configuration options for the power management and operating frequency of the processor's integrated graphics and media engine.

- **RC6 (Render Standby)** – Enables or disables the RC6 low-power state for the integrated graphics render engine. Default: Enabled.
- **MC6 (Media Standby)** – Enables or disables the MC6 low-power state for the integrated media engine. Default: Enabled.
- **Maximum GT Frequency** – Sets the maximum operating frequency of the integrated graphics processor (GT). Default: Maximum.
- **Disable Turbo GT Frequency** – Enables or disables Intel® Turbo frequency for the integrated graphics processor. Default: Disabled.

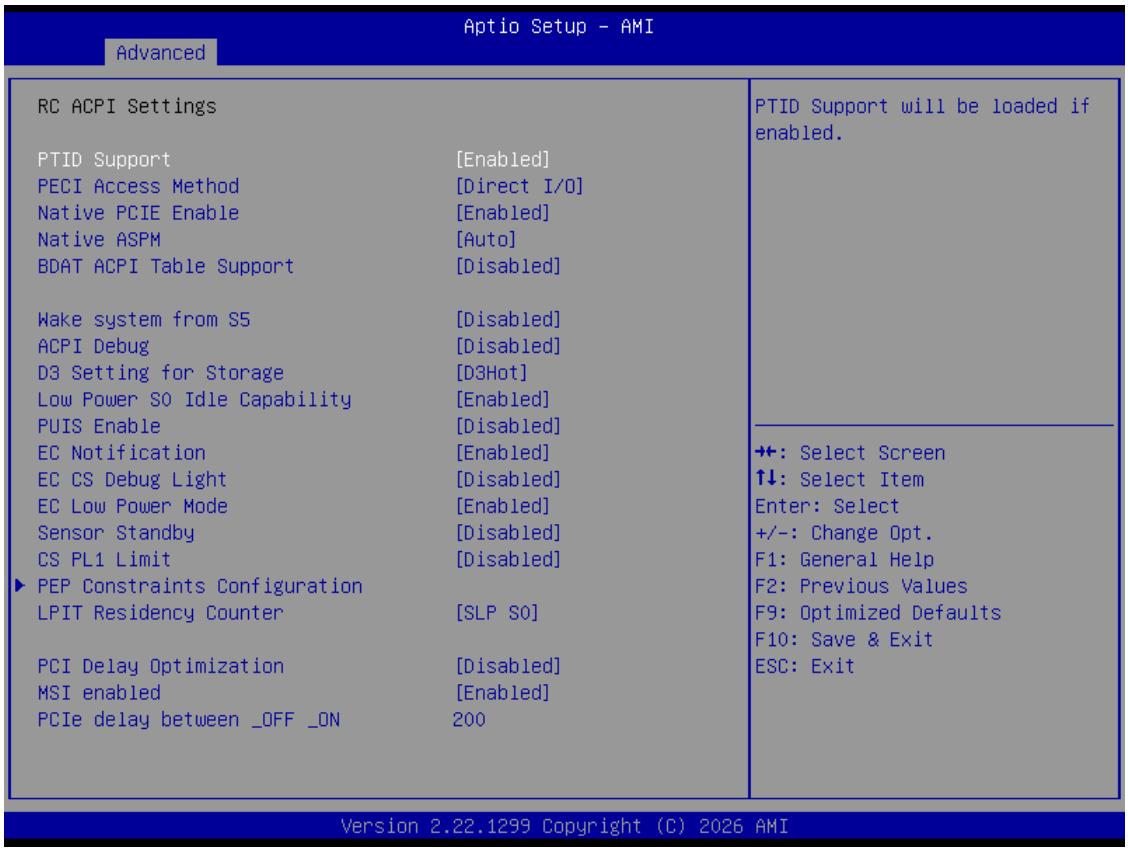
3.3.4 Thermal Configuration



The Thermal Configuration menu provides configuration options for thermal management and system temperature control.

- **Enable All Thermal Functions** – Enables or disables all platform thermal management functions.
- **CPU Thermal Configuration** – Configures processor thermal management settings and thermal protection features.
- **Platform Thermal Configuration** – Configures platform-level thermal management settings.
- **Intel® Innovation Platform Framework Configuration** – Configures Intel® Innovation Platform Framework (IPF) settings for platform thermal, power, and performance management.

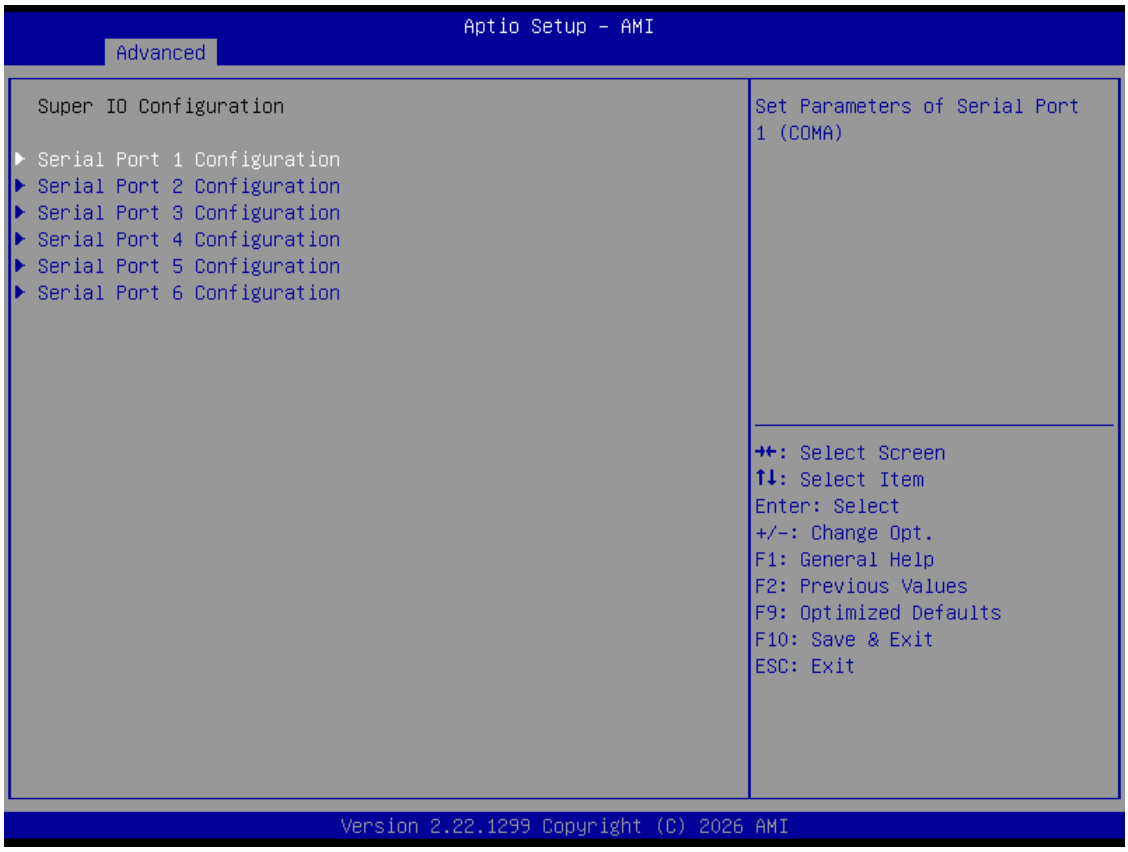
3.3.5 ACPI Setting



The ACPI Settings menu provides configuration options for Advanced Configuration and Power Interface (ACPI) power management features.

- **Wake System from S5** – Enables or disables system wake-up from the S5 (Soft Off) power state.

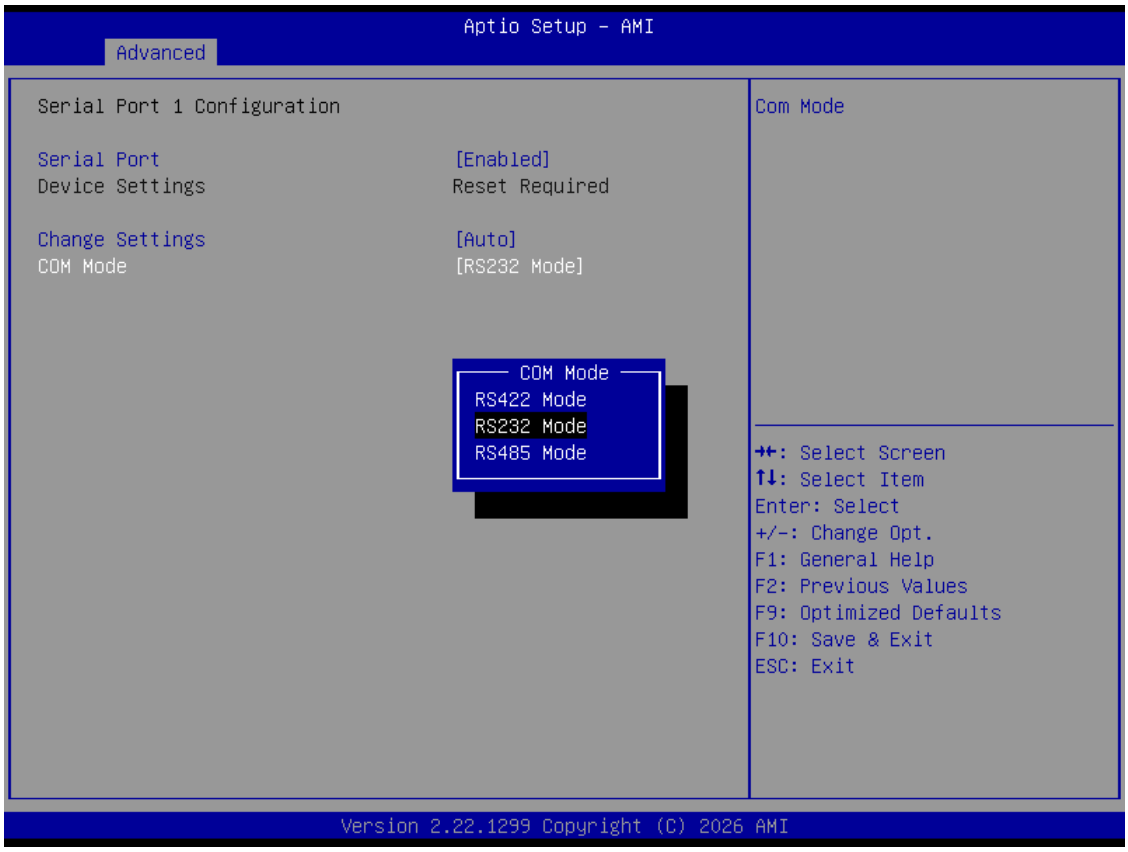
3.3.6 Super IO Configuration



Serial Port 1~6 Configuration

- **Serial Port:** Enable or disable serial port (COM). Default: Enabled.
- **Device Setting (Read-only):** Displays serial ports' interrupt and location.
- **Change Setting:** Change serial port settings and default setting is recommended as "Auto".

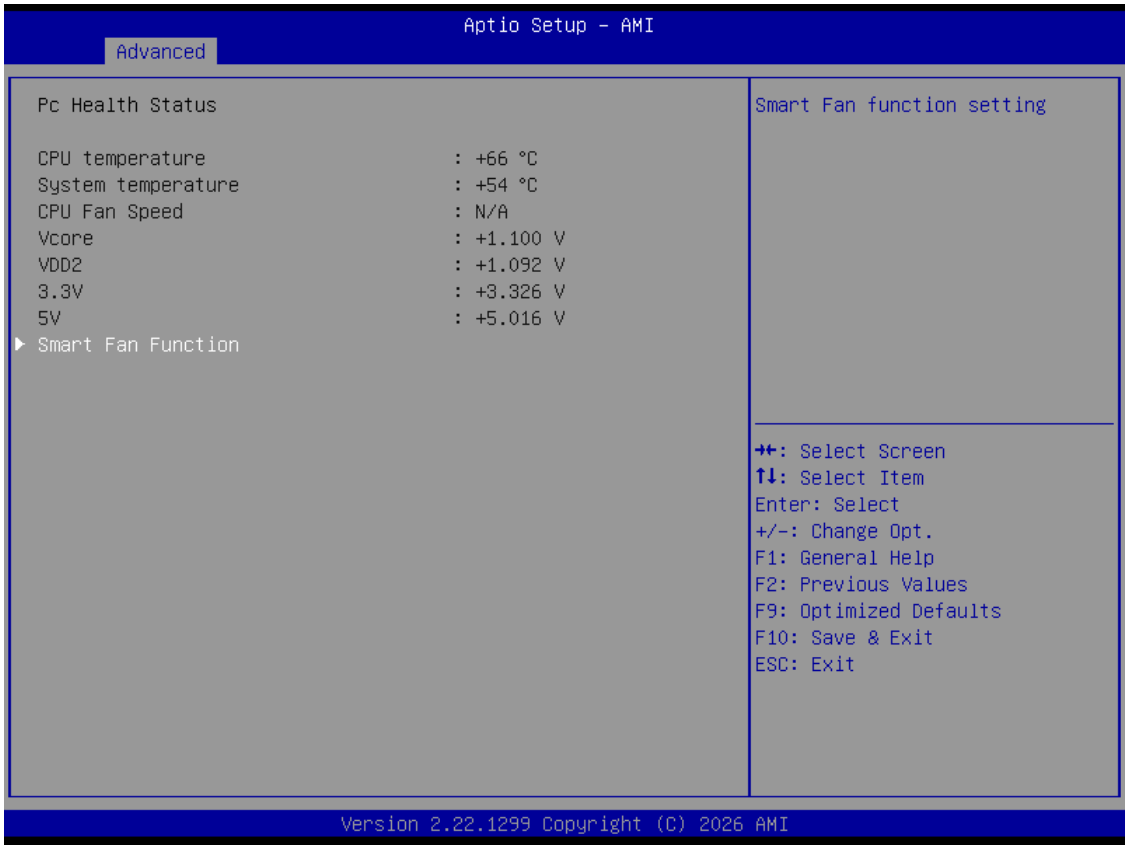
3.3.6.1 COM1/COM2 RS-422 / RS-232 / RS-485 Configuration



Serial Port 1/2 Configuration: To switch communication protocols, enter Serial Port 1/2 Configuration, locate the COM Mode option, and select the desired protocol: RS232, RS485, or RS422. The default setting is RS232.

- **Serial Port:** Enables or disables the onboard serial port. Enabled by default.
- **Device Settings:** Displays the current I/O address and interrupt (IRQ) assigned to the selected serial port.
- **Change Settings:** Changes the serial port configuration. It is recommended to keep the default setting, auto.
- **COM Mode:** Selects the communication mode for COM1 and COM2. The following modes are supported:
  - RS-422 Mode
  - RS-232 Mode (Default)
  - RS-485 Mode

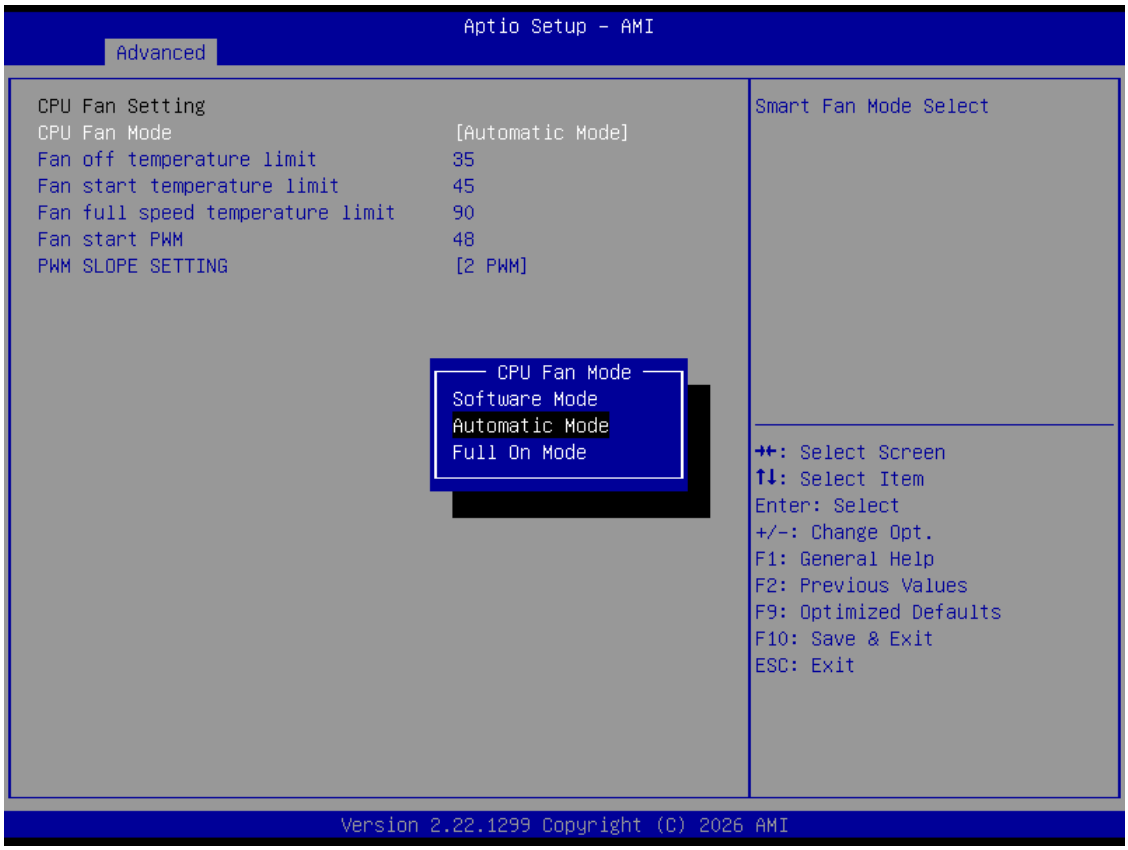
3.3.7 Hardware Monitor



PC Health Status: The PC health status displays CPU temperature, system temperature, fan speed, and other relevant voltage values. The above parameters have a certain range, and the system cannot run beyond these ranges.

1. CPU Temperature
2. System Temperature
3. CPU Fan Speed: Displays the current CPU fan speed.
4. VCore: +1.100V (CPU core voltage)
5. VDD2: +1.225V (RAM voltage)
6. 3.3V: +3.3V (Power Supply voltage)
7. 5V: +5V (Storage devices and USB ports voltage)
8. Smart Fan Function: CPU Fan Setting

3.3.8 Smart Fan Function/CPU Fan Setting



Advanced → PC Health Status → Smart Fan Function → CPU Fan Setting → CPU Fan Mode

CPU Fan Mode: The CPU Fan Setting menu allows you to configure the CPU fan control mode and temperature thresholds. Selects the CPU fan control mode.

- **Software Mode** – Allows manual configuration of the fan control parameters, including the temperature thresholds and PWM duty cycle.
- **Automatic Mode (Default)** – Automatically adjusts the fan speed according to the CPU temperature.
- **Full On Mode** – Runs the CPU fan at full speed continuously for maximum cooling.

Fan Off Temperature Limit: the temperature threshold below which the fan stops.

Fan Start Temperature Limit: the temperature at which the fan starts operating.

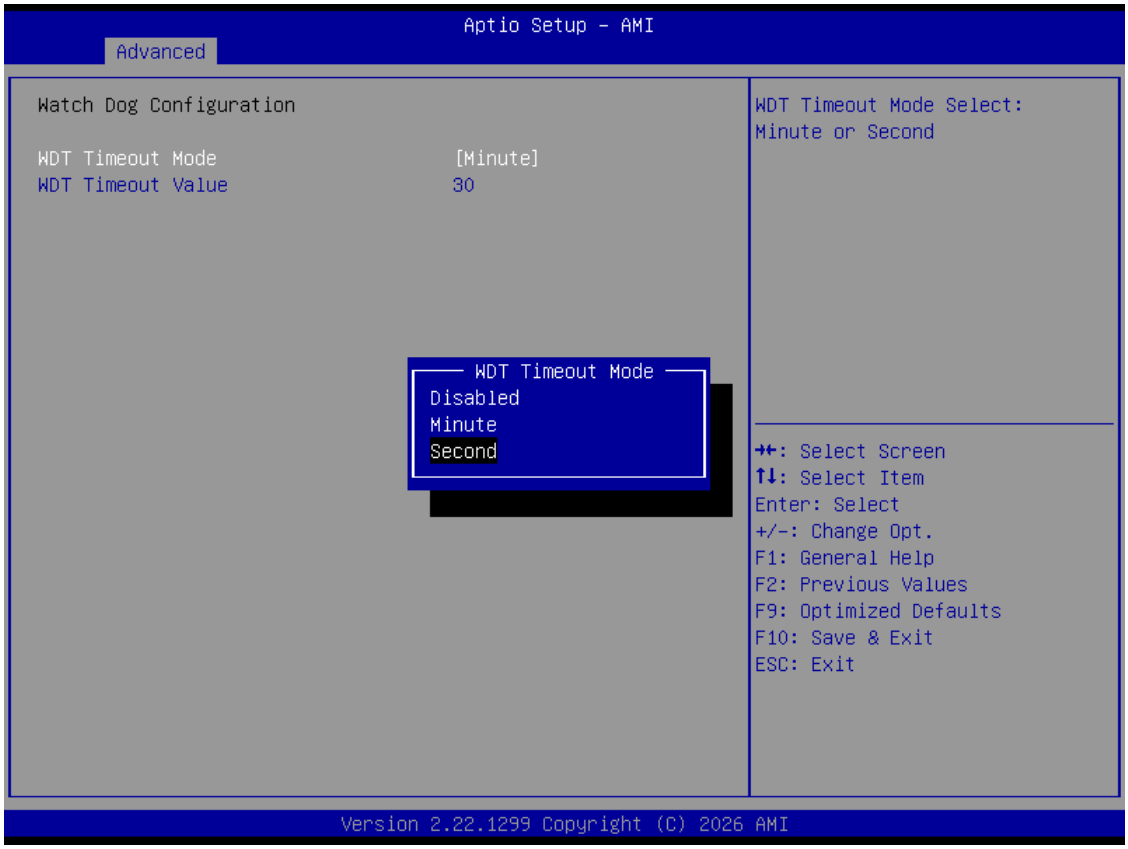
Fan Full Speed Temperature Limit: the temperature at which the fan runs at full speed.

Fan Start PWM: the initial PWM duty cycle when the fan starts.

PWM Slope Setting: Adjusts the rate at which PWM duty cycle increases with temperature.

Note: This option may display N/A depending on the selected fan control mode or platform configuration

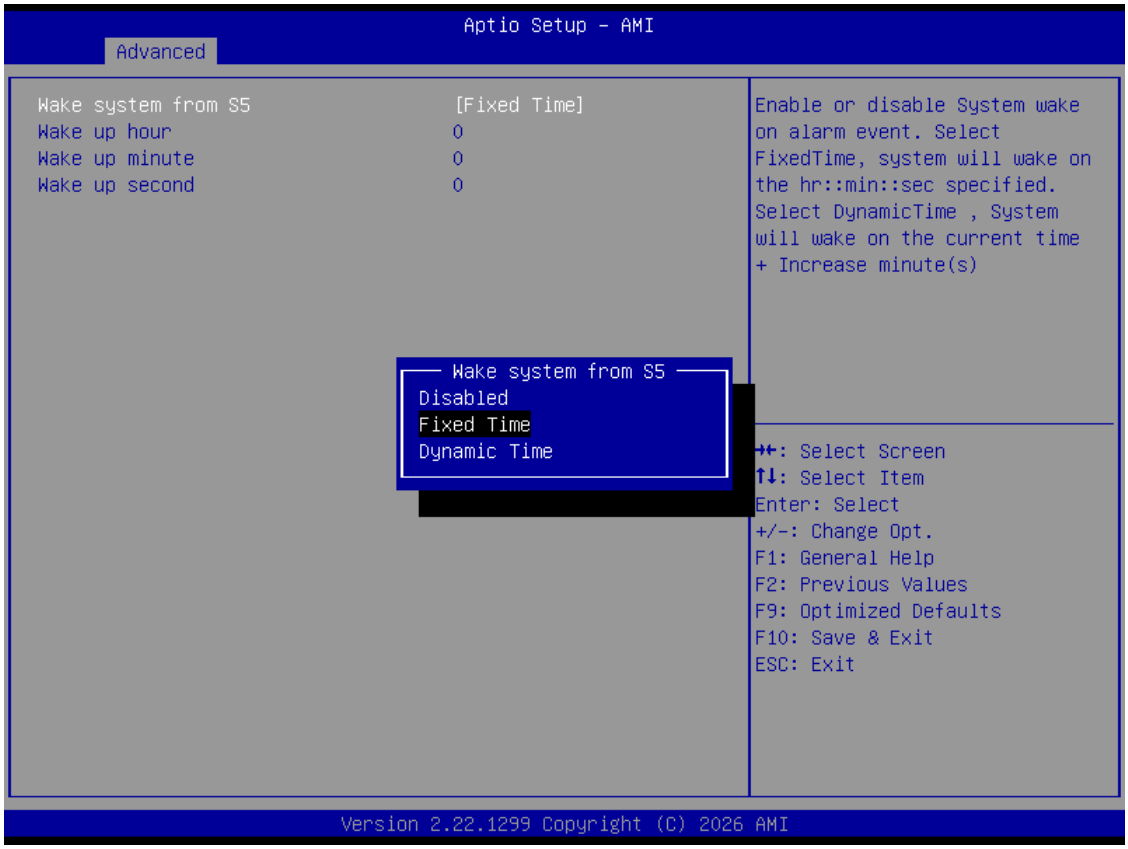
3.3.9 Watch Dog Configuration



Watch Dog Configuration

- WDT Timeout Mode: Select Minute or Second

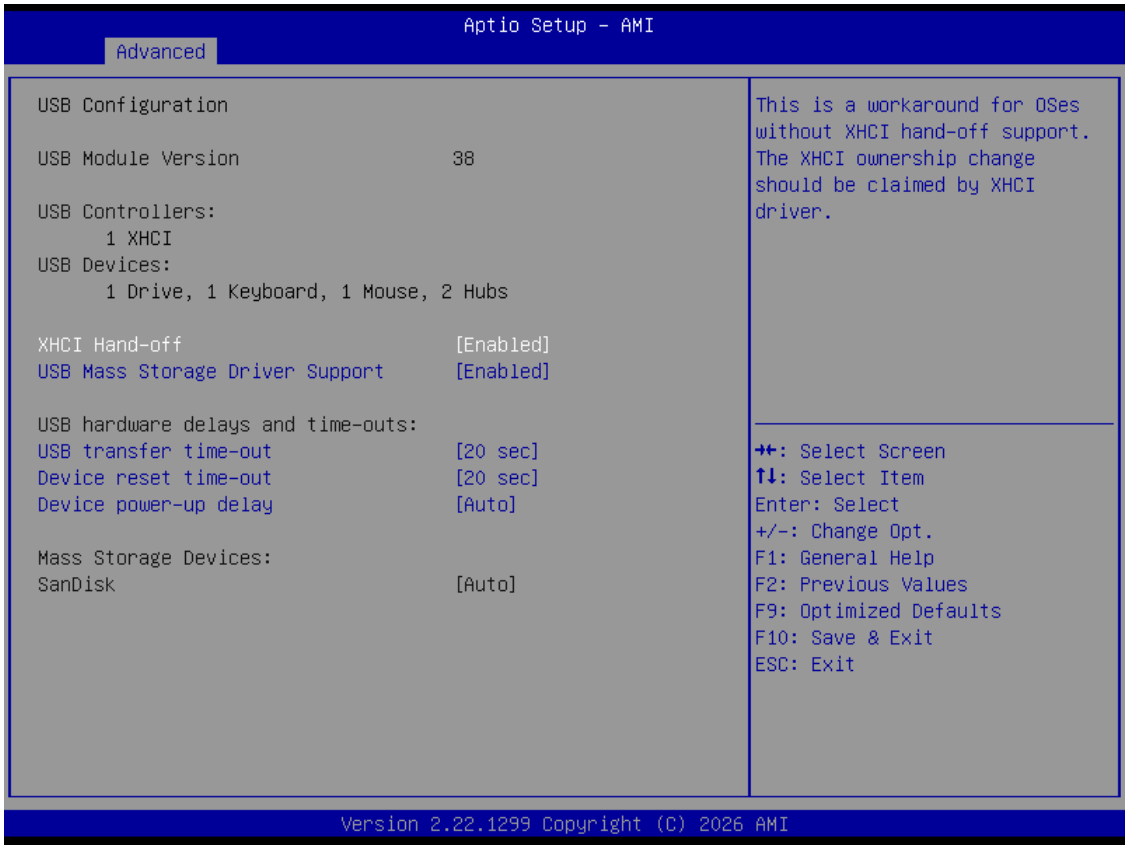
3.3.10 S5 RTC Wake Settings



S5 RTC Wake Settings

- **Wake System from S5**: Enables or disables automatic system power-on from the S5 (shutdown) state.
  Default: Disabled
- **Wake Time Mode**: Selects the wake-up timing mode.
  - **Fixed Time**: When selected, the system wakes at the specified **Hour : Minute : Second**.
  - **Dynamic Time**: When selected, the system wakes after a dynamically calculated time interval.

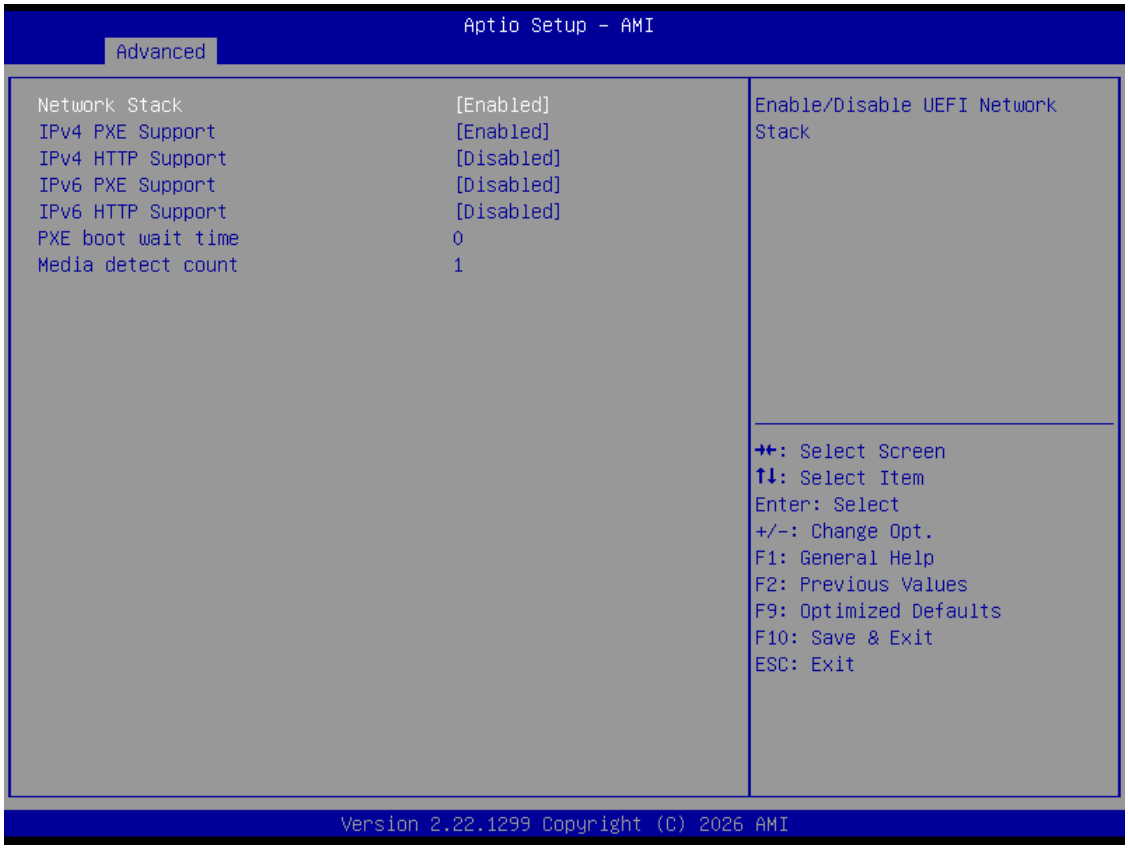
3.3.11 USB Configuration



The USB Configuration menu provides configuration options for the onboard USB controller, USB storage devices, and USB timing parameters.

- **XHCI Hand-off** – Enables or disables the operating system hand-off of the USB XHCI controller.
- **USB Mass Storage Driver Support** – Enables or disables support for USB mass storage devices. Default: Enabled.
- **USB Hardware Delays and Time-outs** – Configures USB hardware timing and timeout parameters.
- **USB Transfer Time-out** – Sets the timeout value for USB control, bulk, and interrupt transfers. Default: 20 seconds.
- **Device Reset Time-out** – Sets the timeout value for USB mass storage device reset operations. Default: 20 seconds.
- **Device Power-up Delay** – Sets the maximum delay allowed for a USB device to become ready after power is applied.

3.3.12 Network Stack Configuration

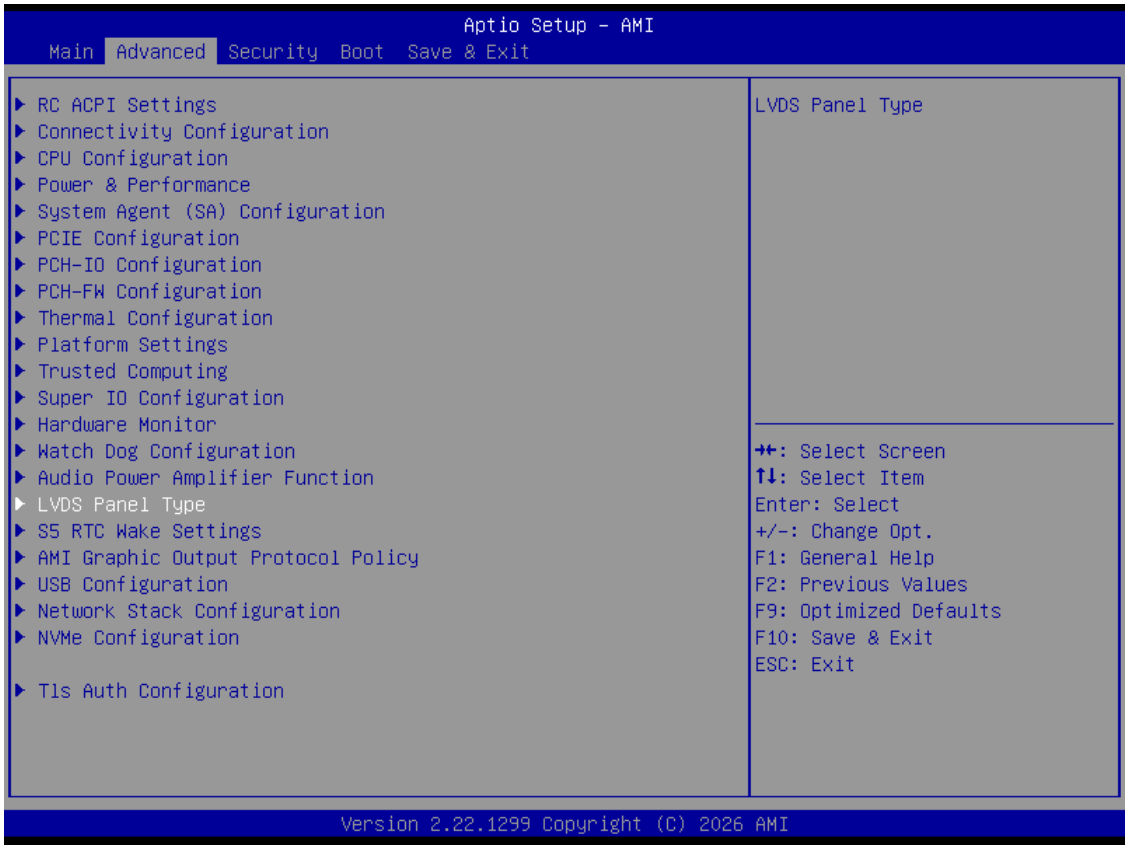


The Network Stack controls UEFI network boot (PXE/HTTP) and is disabled by default.

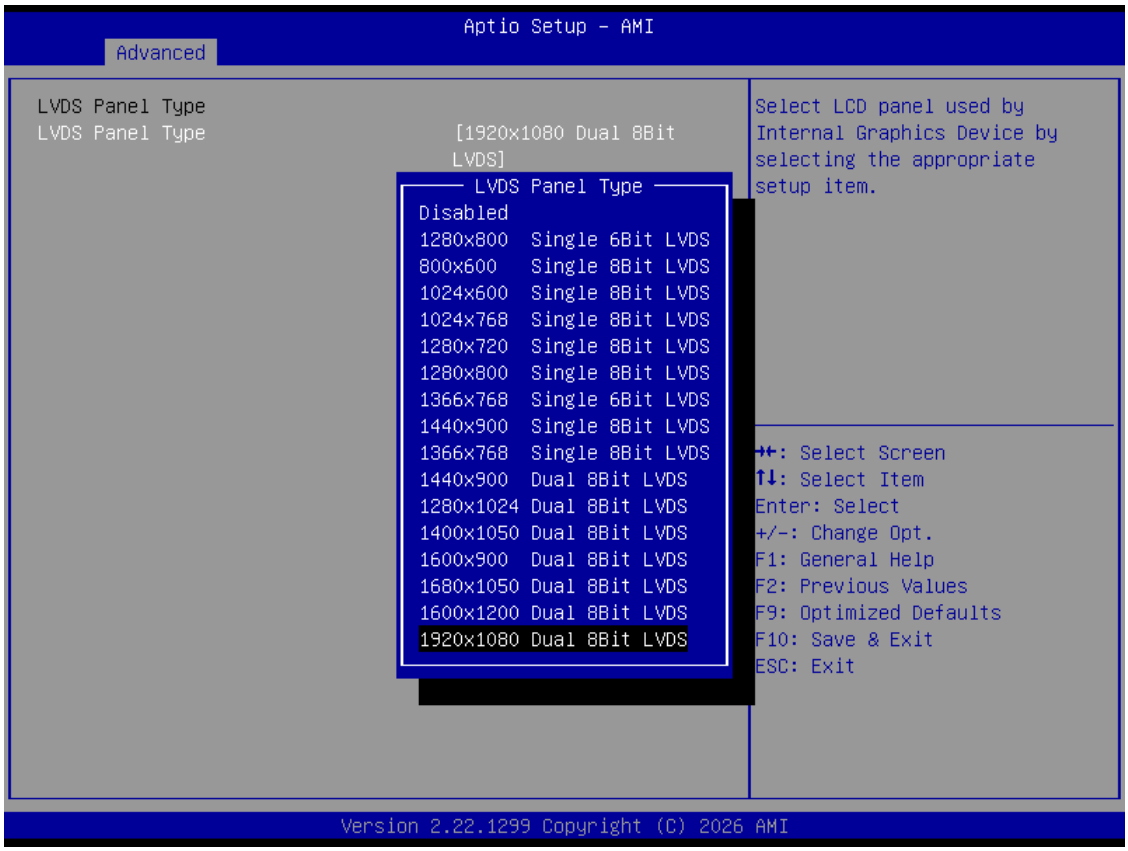
- **IPv4 PXE Support:** PXE boot over IPv4
- **IPv4 HTTP Support:** HTTP boot over IPv4
- **IPv6 PXE Support:** PXE boot over IPv6
- **IPv6 HTTP Support:** HTTP boot over IPv6
- **PXE Boot Wait Time:** Timeout delay for PXE boot
- **Media Detect Count:** Retry count for network device detection

3.3.13 Steps to Configure LVDS in BIOS

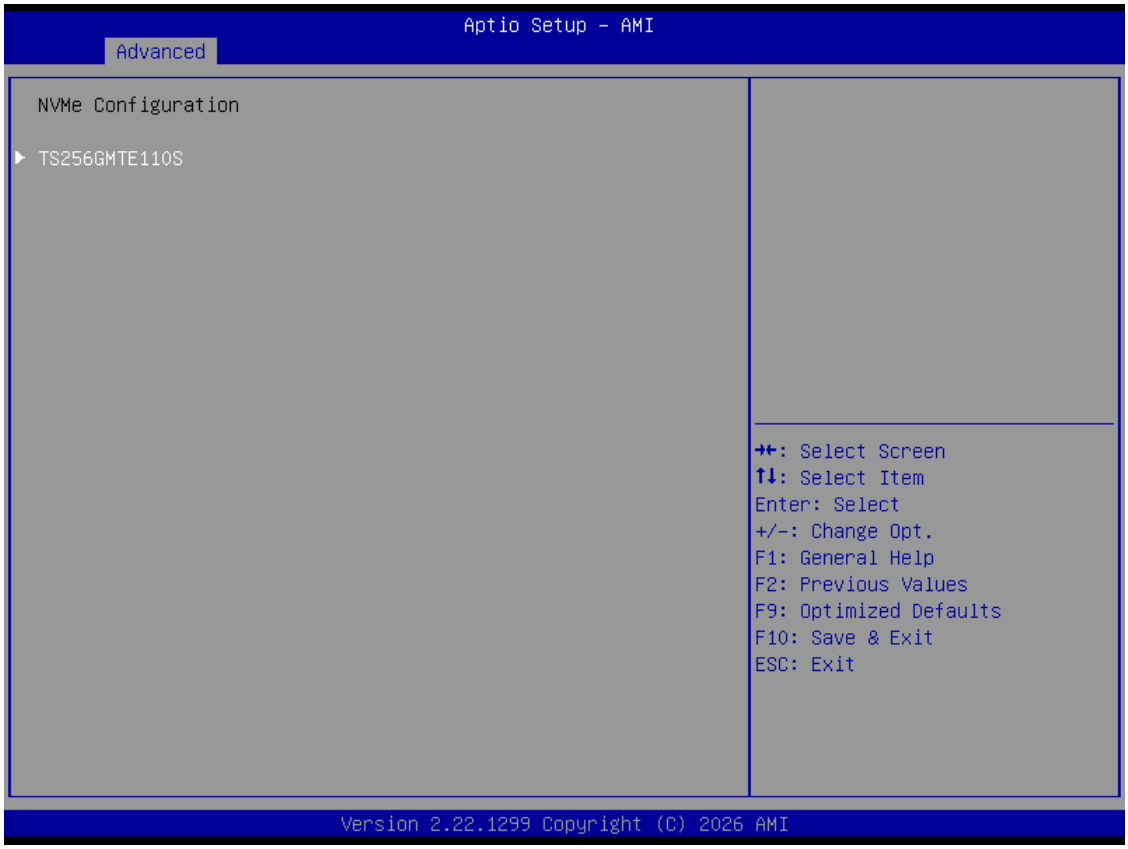
1. During system startup, press **<Delete>** to enter the BIOS Setup Utility. Navigate to **Advanced → LVDS Panel Type**, then press **<Enter>** to open the configuration menu, as shown below.



2. Select **LVDS Panel Type**. The default setting is **Disabled**, which disables the LVDS interface. Select the appropriate resolution, color depth, and LVDS channel configuration according to the specifications of the connected LCD panel. *(Note: Please refer to the LCD panel datasheet for the supported resolution, color depth, and LVDS interface configuration before selecting the corresponding LVDS panel type.)*

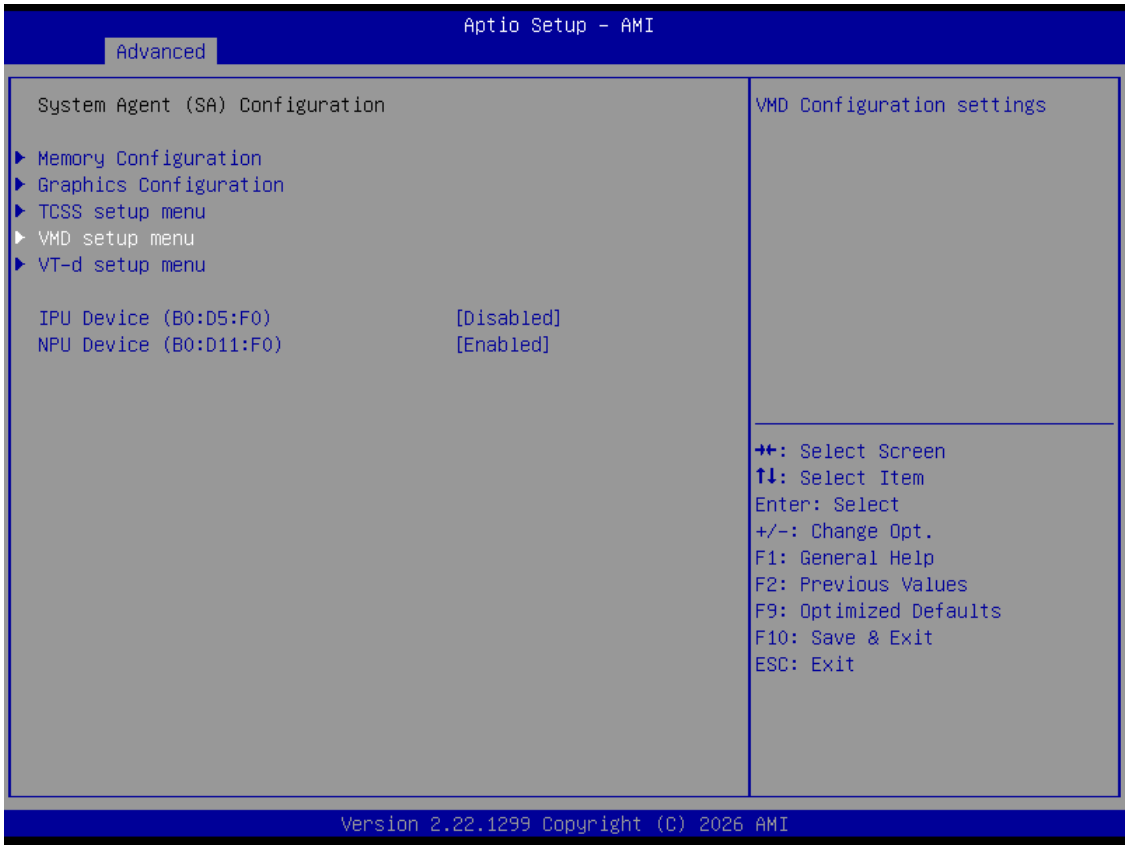


3.3.14 NVME Configuration



When an NVMe SSD is installed, this menu displays information such as the drive model and storage capacity.

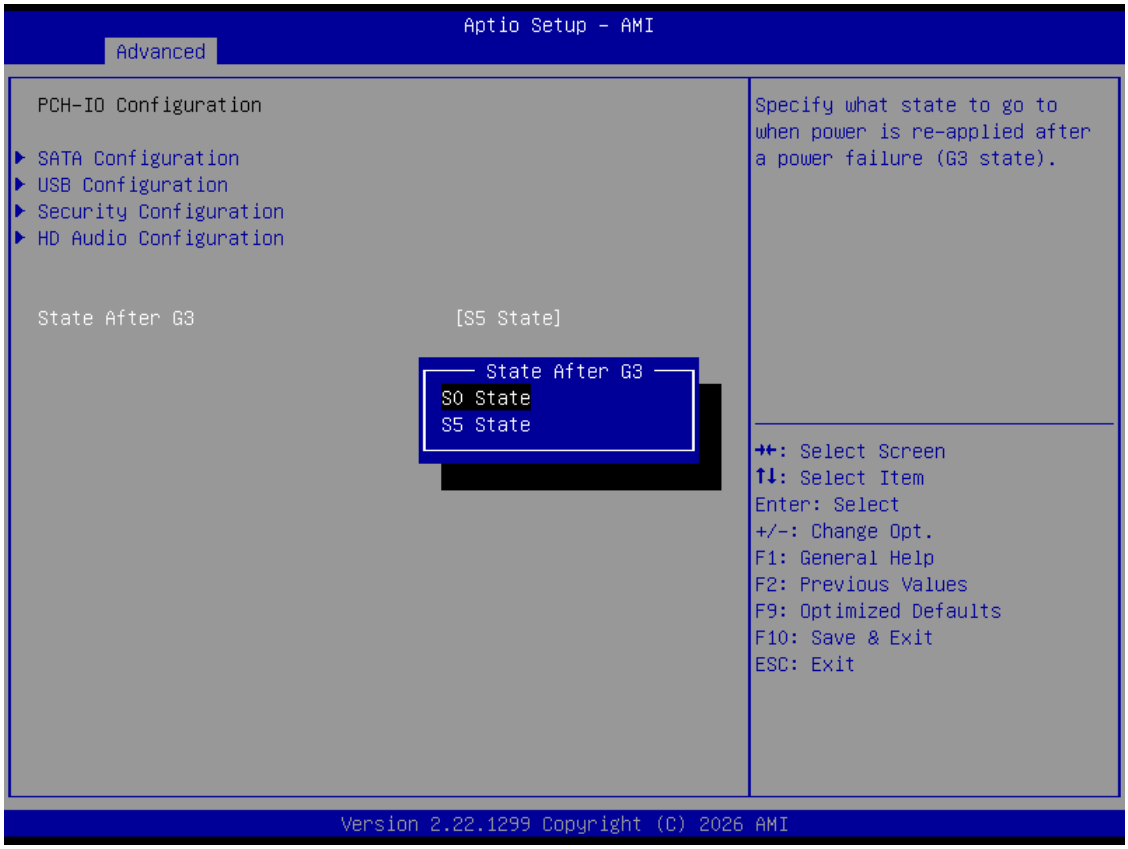
3.3.15 System Agent (SA) Configuration



The System Agent (SA) Configuration menu provides configuration options for system memory, integrated graphics, display interfaces, virtualization, and platform devices.

- **Memory Configuration** – Configures system memory settings.
- **Graphics Configuration** – Configures the integrated graphics controller and display settings.
- **TCSS Setup Menu** – Configures Intel® Thunderbolt™ and USB Type-C® Subsystem (TCSS) settings.
- **VMD Setup Menu** – Configures Intel® Volume Management Device (VMD) settings, including RAID support for compatible storage devices.
- **VT-d Setup Menu** – Configures Intel® Virtualization Technology for Directed I/O (VT-d).
- **IPU Device** – Enables or disables the Intel® Image Processing Unit (IPU). Default: Disabled.
- **NPU Device** – Enables or disables the Intel® Neural Processing Unit (NPU). Default: Enabled.

3.3.16 State After G3



The **State After G3** (AC Power Recovery) option configures the system power state after AC power is restored following a power failure (G3 state). It is located under:

PCH-IO Configuration

- **SATA Configuration** – Configures SATA controller settings.
- **USB Configuration** – Configures USB controller and device settings.
- **Security Configuration** – Configures security-related settings.
- **HD Audio Configuration** – Configures onboard HD Audio settings.
- **State After G3** – Selects the system power state after AC power is restored.

Available options:

- **S0 State** – Automatically powers on the system when AC power is restored.
- **S5 State** – Keeps the system powered off after AC power is restored. Default.

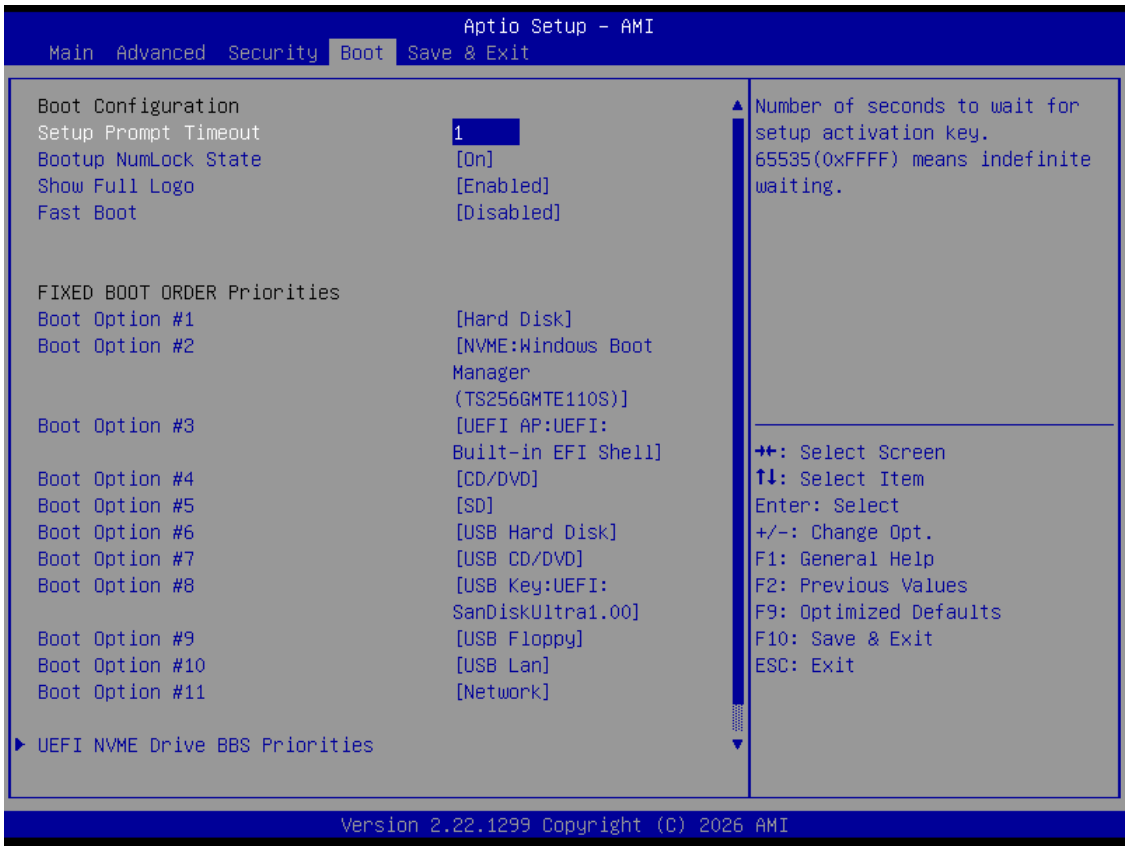
3.4 Security

Administrator Password: Set the Administrator Password.

User Password: Set User Password.

Secure Boot: Secure boot

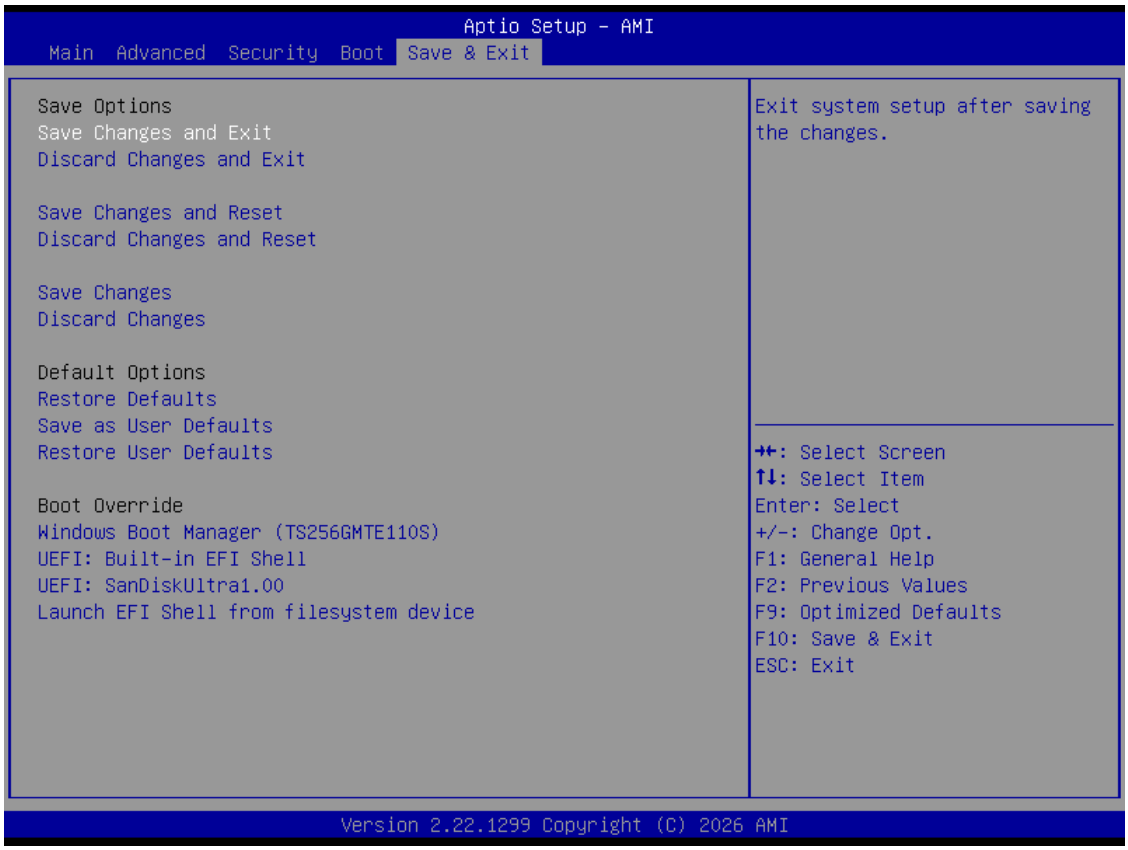
3.5 BOOT



The Boot menu provides configuration options for system startup behavior, boot device priority, and UEFI boot settings.

- **Setup Prompt Timeout –** Sets the number of seconds the system waits for the BIOS Setup key <Delete> to be pressed during startup.
- **Bootup NumLock State** – Enables or disables the Num Lock function during system startup. Default: On.
- **Show Full Logo –** Enables or disables the display of the full-screen manufacturer logo during POST. Default: Enabled.
- **Fast Boot –** Enables or disables Fast Boot to reduce system startup time. Default: Disabled.
- **Boot Option #1–#11 –** Configures the boot priority order of available boot devices.
- **UEFI NVMe Drive BBS Priorities –** Configures the boot priority of UEFI NVMe storage devices.
- **UEFI Application Boot Priorities –** Configures the boot priority of UEFI applications.

3.7 Save & Exit



Save Changes and Exit:

Exit the system setup after saving the changes and continue to start the computer.

Discard Changes and Exit:

Exit the system setup without saving any changes and continue to start the computer.

Save Changes and Reset:

Reset the system after saving the changes.

Discard changes and Reset:

Reset the system without saving any changes.

Save Changes:

Save changes done so far to any of the options.

Discard Changes:

Discard changes done so far to any of the options.

Restore Defaults:

Restore/load default values for all the options.

Save as User Defaults:

Save the changes done so far as the user defaults.

Restore User Defaults:

Restore the user defaults to all the options.

Boot Override:

Boot device selection can override your boot priority. Select the specified boot device such as SATA, USB Flash Disk, EFI Shell, PXE, etc., and boot directly.

Appendix

GPIO Setting

Accessing GPIO70:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x01); //Bit0=1 set as output，bit0=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x01); // When set as output, Bit0 of I/O address 0xA06 = 1 outputs high level, Bit0 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit0=1 Set as output，bit0=0 Set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); //When set as input, Bit0 of I/O address 0xA06 reflects the read state.

Accessing GPIO71:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x02); // Bit1=1 set as output，bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x02); // When set as output, Bit1 of I/O address 0xA06 = 1 outputs high level, Bit1 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); // Bit0=1 set as output，bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit1 of I/O address 0xA06 reflects the read state.

Accessing GPIO72:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x04);    //Bit2=1 set as output，bit2=0 set as input
WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x04); // When set as output, Bit2 of I/O address 0xA06 = 1 outputs high level, Bit2 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit2 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO73:

Example: Accessing via IO

Set as output：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x08); //Bit3=1 set as output，bit3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x08); // When set as output, Bit3 of I/O address 0xA06 = 1 outputs high level, Bit3 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit3=1 set as output，bi3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit3 of I/O address 0xA06 reflects the read state.

Accessing GPIO74:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x10); //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x10); // When set as output, Bit4 of I/O address 0xA06 = 1 outputs high level, Bit4 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit4 of I/O address 0xA06 reflects the read state.

Accessing GPIO75:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x20);    //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x20); // When set as output, Bit5 of I/O address 0xA06 = 1 outputs high level, Bit5 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit5 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO76:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x40); //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x40); // When set as output, Bit6 of I/O address 0xA06 = 1 outputs high level, Bit6 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit6 of I/O address 0xA06 reflects the read state.

Accessing GPIO77:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x80);    //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x80); // When set as output, Bit7 of I/O address 0xA06 = 1 outputs high level, Bit7 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit7 of I/O address 0xA06 reflects the read state.
```