User Manual

AL10 V2.0

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AL10 User Manual

(Version 2.0)

Release Notes:

No.	Description	Date
V2.0	• LVDS controller updated from RTL2136 to CS5211, supporting BIOS-level display parameter configuration. • Added 19V input version. • Added M.2 W/S slot supporting M.2 2242 SATA or M.2 3042 4G modules. • Network chipset upgraded from Intel i225V to Intel i226V. • PANEL interface (eDP/DP/HDMI) is now optional. • Added CASEOPEN chassis-intrusion pin. • Added HDMI HPD Lock support. • Onboard buzzer optional	2025/7/06
V1.0	Initial version	2022/7/20

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Warning

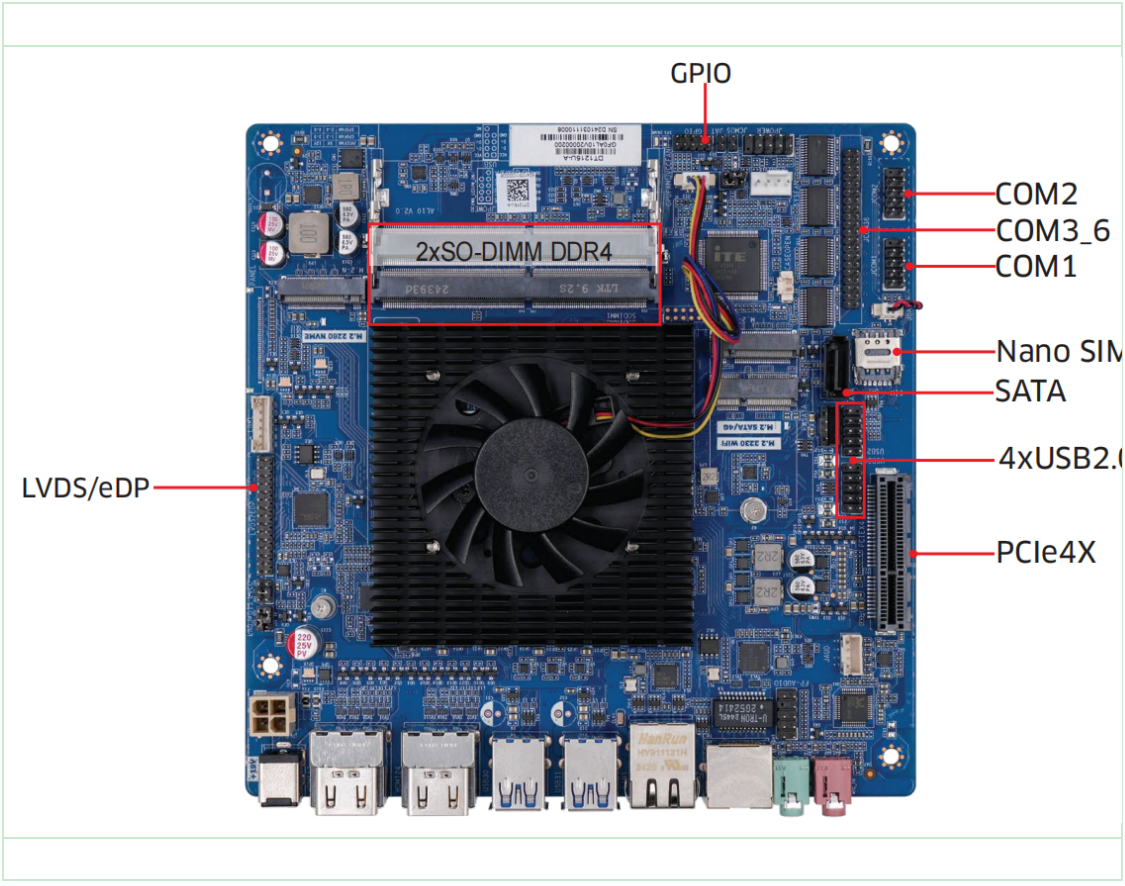
1. Before using the product, carefully read the manual to ensure proper installation and operation.
2. If you are not ready to install any extension card, store it in an anti-static protective bag to prevent damage.
3. To discharge any static electricity, briefly touch a grounded metal object before removing the extension card from the protective bag.
4. Always wear anti-static gloves and handle the card by its edges to avoid damaging sensitive components.
5. Verify that the power supply voltage is correct before connecting the motherboard to the power supply.
6. To prevent electric shock or damage, always turn off the AC power or unplug the power cord before removing or reconfiguring the motherboard or any components.
7. Unplug the AC power cord from the outlet before relocating the motherboard or any components.
8. Ensure all power cords are unplugged before connecting or disconnecting any equipment to avoid electrical hazards.
9. Wait at least 30 seconds after powering off the system before powering it on again to prevent unnecessary wear.
10. If any issues arise during operation, consult a qualified professional for assistance.
11. This product may cause radio interference in certain environments; if necessary, users should take appropriate measures to mitigate such interference.

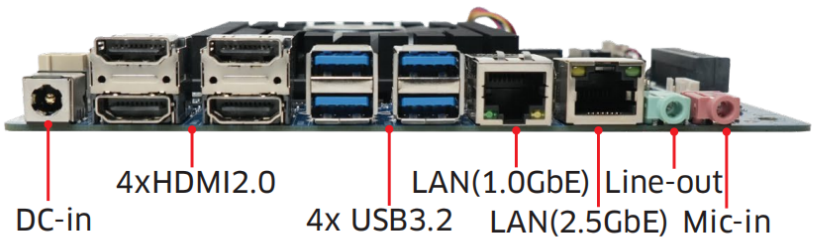
Contents

Chapter 1 Product Introduction

1.1 Brief Introduction

The AL-10 V2.0 is a mini ITX motherboard based on the Intel Alder Lake series processor; features a small form factor, low power consumption, and high performance.





1.2 Parameters

CPU:

CPU	Cores/Threads	Base Frequency	Max Turbo Frequency	Cache	TDP
Intel i3-1215U	6C(2E+4P)/8T	1.2 GHz	4.40GHz P-Core:4.40GHz E-Core:3.30GHz	10MB	15W Max 55W, Default 15W, PL1/PL2:15W
Intel i5-1235U	10C(2E+8P)/12T	1.3GHz	4.40GHz P-Core:4.40GHz E-Core:3.30GHz	12MB	15W Max 55W, Default 15W, PL1/PL2:15W
Intel i7-1255U	10C(2E+8P)/12T	1.7GHz	4.70GHz P-Core:4.70GHz E-Core:3.50GHz	12MB	15W Max 55W, Default 15W, PL1/PL2:15W
Intel i7-1360P	12C(4E+8P)/16T	2.2GHz	5.00GHz P-Core:5.00GHz E-Core:3.70GHz	18MB	28W Max 64W, Default 28W, PL1/PL2:28W

GPU:

CPU	GPU Name	Max Dynamic Frequency	Execution Units
Intel i3-1215U	Intel® UHD Graphics for 12th Gen Intel® Processors	1.10 GHz	64EU
Intel i5-1235U	Intel® Iris® Xe Graphics eligible	1.20 GHz	80EU
Intel i7-1255U	Intel® Iris® Xe Graphics eligible	1.25 GHz	96EU
Intel i7-1360P	Intel® Iris® Xe Graphics eligible	1.50 GHz	96EU

Display Interfaces: Supports 4 HDMI 2.0 ports, 1 LVDS port (labeled EDP/LVDS onboard, 2.0 mm, default LVDS with optional eDP), and 1 optional PANEL multifunction port supporting eDP/DP/HDMI.

Memory: 2x SO-DIMM DDR4-3200, supports dual-channel, maximum capacity: 64GB

Storage/Expansion:

- 1xM.2 Key M slot (labeled: M.2_N1/2) supporting 2280 NVMe SSDs
- 1xM.2 Key B slot (labeled: M.2_WS) supporting 2242 SATA SSDs or 3042 4G modules
- 1xSATA 3.0 port (labeled: SATA)
- 1x M.2 Key E slot (labeled: M.2_E) supporting 2230 Wi-Fi & Bluetooth modules (CNVI/PCIe/USB 2.0)
- 1x PCIe x4 slot (labeled: PCIeX4)

Audio: Realtek HD ALC897 High-Definition Audio Codec, support Line_out, Mic_in.

Ethernet: 2x RJ45 Gigabyte Network Controllers.

- LAN1: Intel i219-V, Date Rate Per Port: 1.0GbEs. LAN2: Intel i226-V, Data Rate Per Port: 2.5 GbE.

USB:

- 4xUSB 3.2 Gen 2 Type-A ports (10 Gbps; labeled: USB30/USB31).
- 4xUSB 2.0 Type-A ports (480 Mbps; 2.54 mm header pins routed from USB20/USB21).

Serial COM: 6x COM headers support RS-232 by default (COM1 optionally configurable as RS-485); (labeled: JCOM1/JCOM2 (2.54 mm) and JCOM36 (2.0 mm).

GPIO: 8-bit GPIO (labeled: GPIO, 2.0 mm)

TPM: External TPM module support (Infineon SLB9670, optional).

Buzzer: One onboard buzzer optional (labeled: BUZZ_S)

Others:

- A set of CASEOPEN header (chassis intrusion; labeled: CASEOPEN, 1.25 mm)
- A set of JPOWER header (power pins; labeled: JPOWER, 2.54 mm)
- A set of JAT auto power-on header (hardware auto-start; labeled: JAT, 2.0 mm)
- A set of Front audio header (labeled: F_AUDIO, 2.54 mm)
- A set of Amplifier header (labeled: JAUD, 2.0 mm)
- A set of CPU fan header (4-pin, 5V/12V; labeled: CPU_FAN, 1.25 mm; default 5V cooler)
- A set of System fan header (4-pin, 5V/12V; labeled: SYS_FAN, 2.54 mm)
- A set of Fan voltage select header (5V/12V; labeled: JVCCFAN, 2.0 mm)
- A set of Backlight polarity / LVDS-eDP switch header (labeled: L-ADJ/DIS, 2.0 mm)
- A set of LCD power voltage select header (3.3V/5V/12V; labeled: L-VCC, 2.0 mm)
- A set of Screen backlight power switch header (labeled: L-BKL, 2.0 mm)
- A set of CMOS clear header (labeled: JCMOS, 2.0 mm)
- A set of JBAT connector (CR2032 3V battery; labeled: JBAT, 1.25 mm)
- SIM card slot

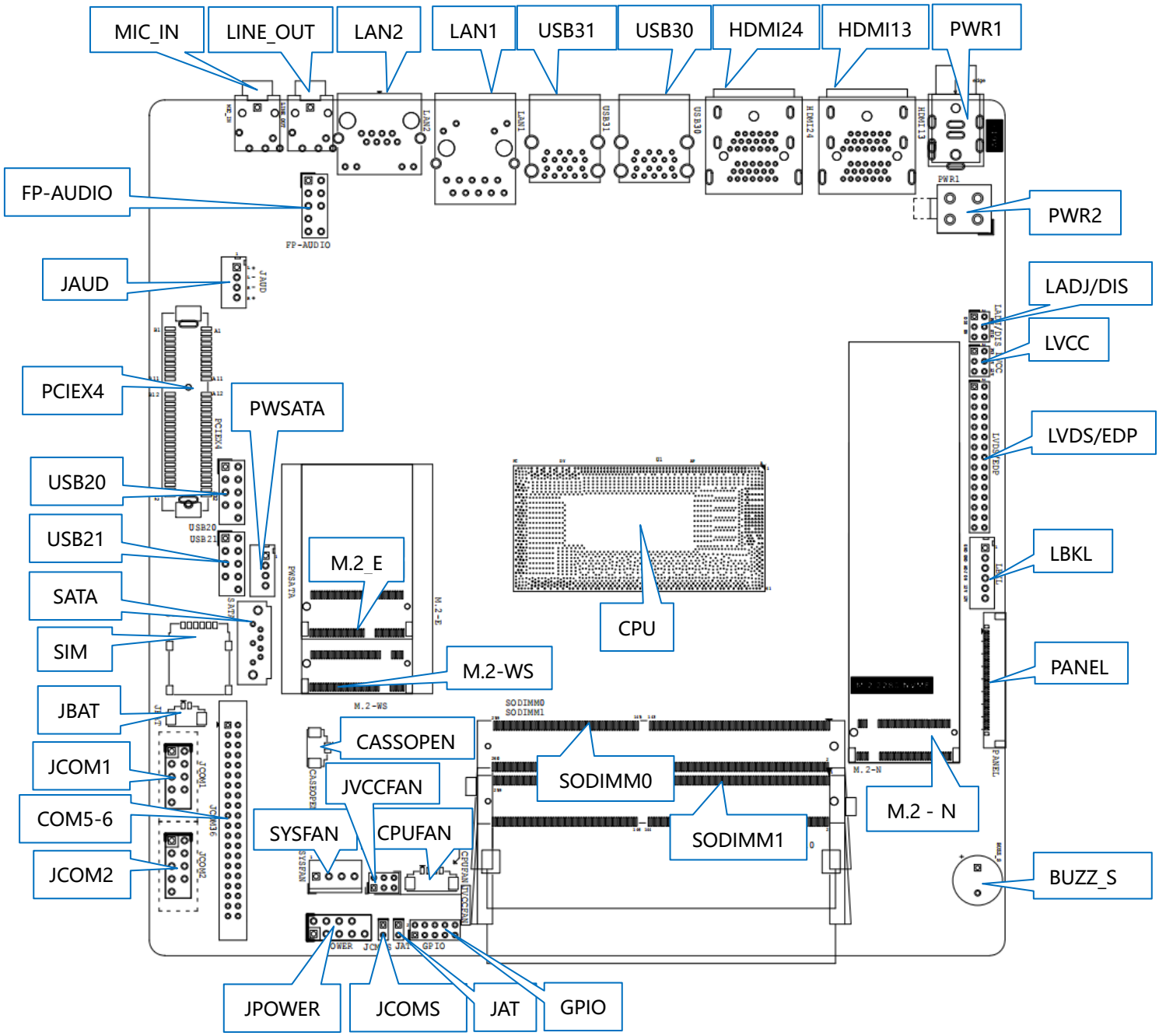
Power: Supports 19V DC (5.5 × 2.5 mm) and 12V DC (5.5 × 2.5 mm) power input options, available as two selectable versions, and includes a 4-pin ATX power input.

Operating Temperature: -20℃~60℃

Form Factor: Mini ITX Motherboard

Dimension: 170mm x 170mm

1.3 Connector Diagram



Chapter 2 Hardware

2.1 Installations

Please refer to the following steps for installation:

1. Read the user manual carefully to make sure all the adjustments on the AL10 are correct.
2. Installing the Memory:
    - Press the ejector tab of the memory slot outwards with your fingertips.
    - Hold the memory module and align the key to the module with that on the memory slot.
    - Gently push the module into the slot until the ejector levers return completely to the closed position, holding the module in place when the module touches the bottom of the slot. To remove the module, press the ejector levers outwards to unseat the module.
3. Installing the expansion cards:
    - Locate the expansion slots and remove the screw, insert the cards into the slot at a 45-degree angle then attach the screw to the expansion cards, gently press down on it then install the screw back.
4. Connect all signal wires, cables, panel control wiring, and power supplies.
5. Start the computer and complete the setup of the BIOS program.

The board's components are integrated circuits and can easily be damaged by Electrostatic Discharge or ESD; therefore, please follow the instructions:

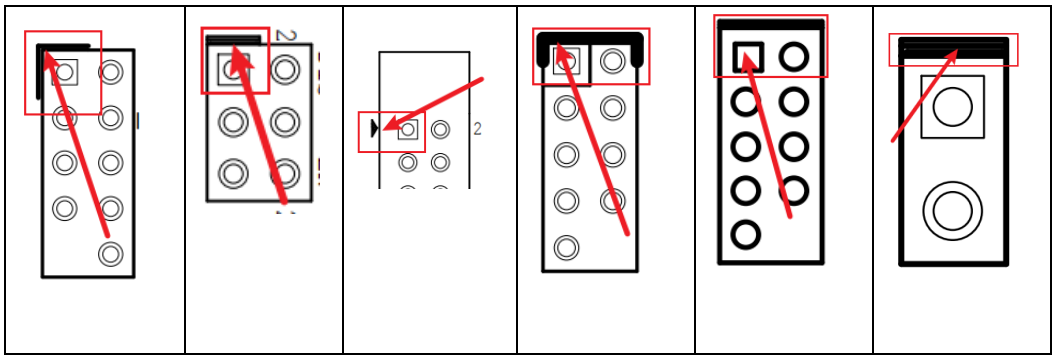
- Hold the board's edge when handing, and do not touch onboard pins, components, or plug sockets.
- When touching integrated circuit components (such as CPU, RAM, etc.), please wear an anti-static wrist strap/glove to avoid electrostatic discharge damage to the board or other sensitive components.
- Before installing the integrated circuits/sensitive components, place the sensitive components in anti-static bags to keep them safe from ESD.
- Please make sure the power switch is OFF before plugging the power plug.

2.2 Jumper Setting

Please configure the jumpers according to your requirements before installing the hardware.

How to identify the first header of jumpers and pins: Observe the mark beside the jumper or pins and find the header marked by “1” or bold line or triangular symbol. Or observe the rear panel and the header with a square solder pad is the first header.

Illustration:



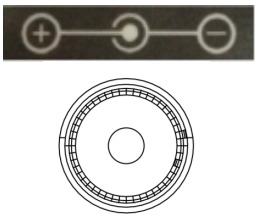
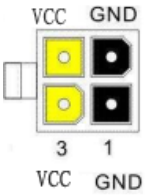
2.3 Memory

The board provides 2x DDR4-3200 MHz SO-DIMM slots, supporting dual-channel with a maximum total capacity of 64 GB.

Note: Ensure the memory module is aligned with the slot key before insertion. When selecting memory, verify that the module meets the required specifications.

2.4 Board Power Supply (Labeled PWR1, PWR2 onboard)

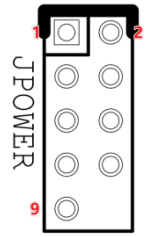
The board supports two DC input versions, selectable as required: 19V DC (5.5 × 2.5 mm) or 12V DC (5.5 × 2.5 mm). An ATX auxiliary power connector (2×2-pin) is also provided.

PWR1: DC power adapter input port	PWR2: ATX supplementary power supply socket (2x2PIN)
	

2.5 Power Switch Socket (Labeled JPOWER onboard)

The JPOWER header serves as the front-panel control interface for connecting the chassis power button, reset button, and indicator LEDs.

Switch Panel Pin Definition:

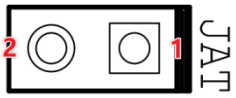


Signal	Pin		Signal
HDD_LED+	1	2	PWR_LED+
HDD_LED-	3	4	PWR_LED-
RSTBTN-	5	6	PWR_ON+
RSTBTN+	7	8	PWR_ON-
NUL	9	10	(Null)

2.6 Hardware Auto Power-On (labeled JAT onboard)

The **JAT** header (labeled **JAT** onboard) controls the hardware power-on auto-start function. Install the appropriate jumper cap to enable or disable this feature.

JAT Settings:

Enable	**Disable**
1-2	NC
	

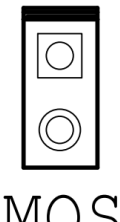
2.7 CMOS Clearance/Retention (labeled CLR_CMOS onboard)

The CMOS is powered by onboard button batteries. Clearing CMOS will permanently remove the previous system settings and restore the board system to original settings (factory settings).

CMOS Clear Procedure:

1. Power off the system completely and disconnect the AC power source.
2. Install a jumper cap on JCMOS pins 1–2 to short the pins and initiate a CMOS clear.
3. Reconnect power and start the system. Press <Del> during POST to enter the BIOS setup.
4. Press F9 to load the default configuration, then save and exit.

JCMOS (Insert the corresponding jumper cap to enable the corresponding function):

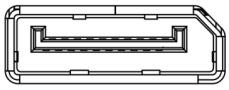
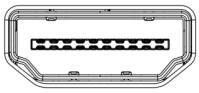
Clear CMOS	NC
1-2	Null
	

⚠ Caution: Do not perform a CMOS clear while the system is powered on. Clearing the CMOS under power may cause permanent damage to the motherboard.

2.8 Display Interfaces

The board provides multiple display outputs, including 1x HDMI, 1x DisplayPort, and 1x LVDS header (optionally configurable as eDP):

- 1 × HDMI 2.0b port supporting up to 4K @ 60 Hz
- 1 × DisplayPort 1.4a port supporting up to 4K @ 60 Hz
- 1 × LVDS header (optional upgrade to eDP) supporting up to 1920 × 1200, 24-bit.
  When configured as an eDP interface (optional), the header supports 3.3 V eDP panels up to 4K @ 30 Hz.

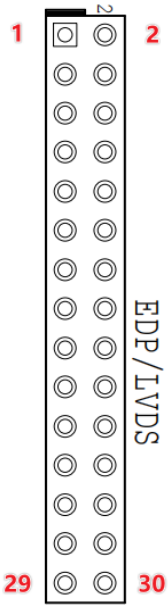
DP1.4a	HDMI2.0b
	

2.8.1 LVDS (labeled EDP/LVDS, L-BKL, L-ADJ/DIS, L-VCC onboard)

When the interface is configured to LVDS mode, the following onboard headers function as LVDS signal, control, and power interfaces. The “EDP/LVDS” header outputs LVDS display signals, while “L-BKL”, “L-ADJ/DIS”, and “L-VCC” provide backlight control, signal configuration, and voltage selection.

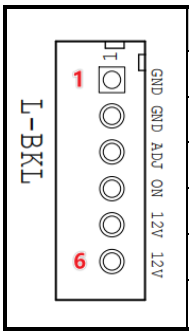
- **EDP/LVDS:** Carries LVDS display signal lines.
- **L-BKL:** Controls LCD backlight on/off and brightness adjustment.
- **L-ADJ/DIS:** Used for LVDS enable/disable control and backlight signal direction (standard/reverse).
- **L-VCC:** Selects the LCD operating voltage.

LVDS Data Pins:



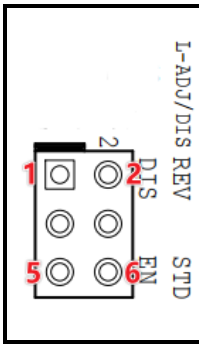
Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	GND
GND	5	6	GND
A_DATA0_DN	7	8	A_DATA0_DP
A_DATA1_DN	9	10	A_DATA1_DP
A_DATA2_DN	11	12	A_DATA2_DP
GND	13	14	GND
A_CLK_DN	15	16	A_CLK_DP
A_DATA3_DN	17	18	A_DATA3_DP
B_DATA0_DN	19	20	B_DATA0_DP
B_DATA1_DN	21	22	B_DATA1_DP
B_DATA2_DN	23	24	B_DATA2_DP
GND	25	26	GND
B_CLK_DN	27	28	B_CLK_DP
B_DATA3_DN	29	30	B_DATA3_DP

LVDS Backlight Connector Pin (Labeled L-BKL onboard):



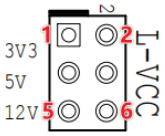
Pin	Signal
1	GND
2	GND
3	LCD_BKL_ADJ
4	LCD_BKL_ON
5	12V
6	12V

LVDS Backlight Adjustment Pin (Standard/Reverse) / LVDS Switch Pin (Labeled L-ADJ/DIS onboard)



Pin	Setting	Function
2-4	Close	REV (Backlight Control Reverse)
4-6	Close	STD (Backlight Control Standard)
1-3	Close	DIS (Disable LVDS)
3-5	Close	EN (Enable LVDS)

LVDS Operating Voltage Adjustment Pin (labeled L_VCC onboard)



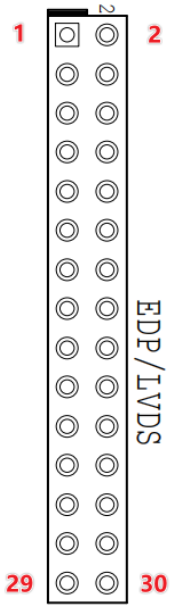
Pin	Setting	Function
1-2	Close	VCC 3.3V
3-4	Close	VCC 5V
5-6	Close	VCC 12V

Caution!!! The LVDS operating voltage adjustment switch is pin controlled. By shorting the jumper caps, the voltage can be flexibly adjusted between 3.3V/5V/12V. Based on your LVDS display's voltage parameters, use the jumper caps to short the pins corresponding to the required voltage. (Do not short pins of different voltages simultaneously.)

2.8.2 eDP (Optional)

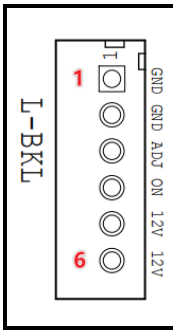
When the interface is configured to eDP mode, the “EDP/LVDS” header outputs eDP signals. The “L-BKL” header is used for panel backlight control, while the “L-ADJ/DIS” header provides backlight signal direction control (standard/reverse). The “L-VCC” header is used to select the panel operating voltage.

eDP Data Pins (labeled EDP/LVDS onboard):



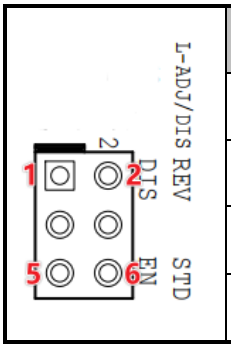
Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	EDP_HPD
GND	5	6	GND
EDP_AUXN	7	8	EDP_AUXP
N/A	9	10	N/A
EDP_DATA0_P	11	12	EDP_DATA0_N
GND	13	14	GND
N/A	15	16	N/A
EDP_DATA1_P	17	18	EDP_DATA1_N
N/A	19	20	N/A
N/A	21	22	N/A
N/A	23	24	N/A
GND	25	26	GND
N/A	27	28	N/A
N/A	29	30	N/A

eDP Backlight Connector Pin (labeled L-BKL onboard):



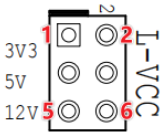
Pin	Signal
1	GND
2	GND
3	LCD_BKL_ADJ
4	LCD_BKL_ON
5	12V
6	12V

eDP Backlight Adjustment Pin (Forward/Reverse)/eDP Switch Pin: (Labeled L-ADJ/DIS onboard)



Pin	Setting	Function
2-4	Close	REV (Backlight Control Reverse)
4-6	Close	STD (Backlight Control Standard)
~~1-3~~	NC	Not Available
~~3-5~~	NC	Not Available

eDP Operating Voltage Adjustment Pin:(labeled L_VCC onboard)

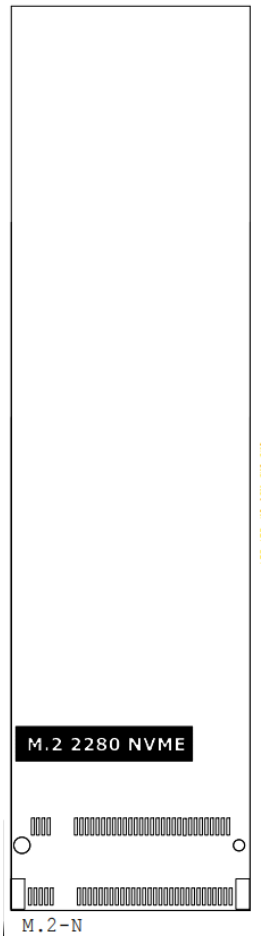
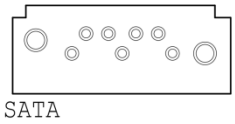


Pin	Setting	Function
1-2	Close	VCC 3.3V
3-4	Close	VCC 5V
5-6	Close	VCC 12V

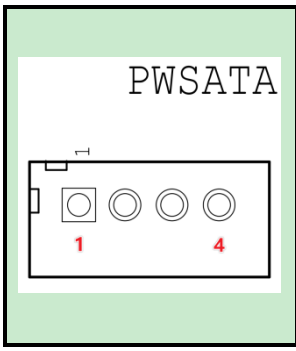
Caution!!! The eDP operating voltage adjustment switch is pin controlled. Jumper caps can be used to flexibly adjust between 3.3V/5V/12V. Based on your eDP display's voltage specifications, use jumper caps to short the pins corresponding to the required voltage. (Do not short pins of different voltages simultaneously.)

2.9 Storage Interfaces (labeled M.2_N/M.2_WS/SATA onboard)

- 1 × M.2 Key M slot (labeled M.2_N onboard) supporting 2280 NVMe SSDs
- 1 × M.2 Key B slot (labeled M.2_WS onboard) supporting 2242 SATA SSDs or 3042 4G modules
- 1 × SATA 3.0 connector (labeled SATA onboard)

M.2_SW5G	M.2_WS	SATA
		

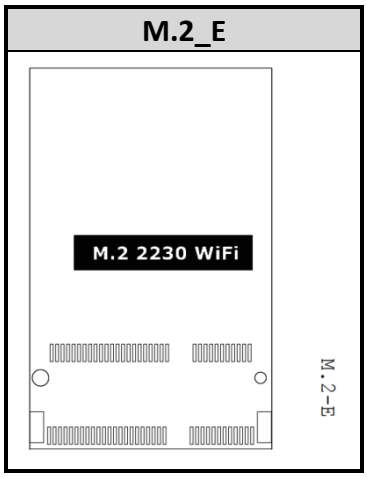
1 x PWSATA 4-pin power connector: (labeled PWSATA onboard)



Pin	Signal
1	5V
2	GND
3	GND
4	12V

2.10 Expansion Slots(labeled M.2_E, PCIEX4 onboard)

- 1 × M.2 Key E slot, supporting 2230 Wi-Fi & Bluetooth modules (CNVI / PCIe / USB 2.0); labeled M.2_E onboard.
- 1 × PCIe x4 slot; labeled PCIeX4 onboard



2.11 USB Interface （labeled USB30, USB31, USB20, USB21 onboard)

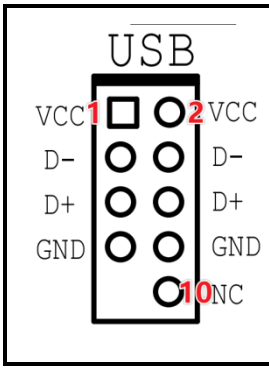
The board provides the following USB ports:

- 4 × USB 3.2 Gen 2 Type-A ports (10 Gbps) — labeled USB30 / USB31 onboard
- 4 × USB 2.0 Type-A ports (480 Mbps) — labeled USB20 onboard (2.54 mm pin headers routed from USB20 / USB21)

The rear USB 3.2 Gen 2 Type-A ports (USB30 / USB31) are powered by the 5V system rail, controlled by the CPU S5 power signal. These ports support system wake-up from sleep/hibernation via a USB keyboard or mouse and supply 5V / 1A to external devices. Notes:

1. Windows 10 or later: If Fast Startup is enabled, the USB30/USB31 ports remain powered after shutdown. If Fast Startup is disabled, the ports lose power after shutdown.
2. Linux: USB30/USB31 ports lose power after shutdown.
3. BIOS Setting: The BIOS allows configuring USB30 power retention after shutdown, independent of the operating system's power state.

USB Pin Definition:(labeled USB20 / USB21 onboard)



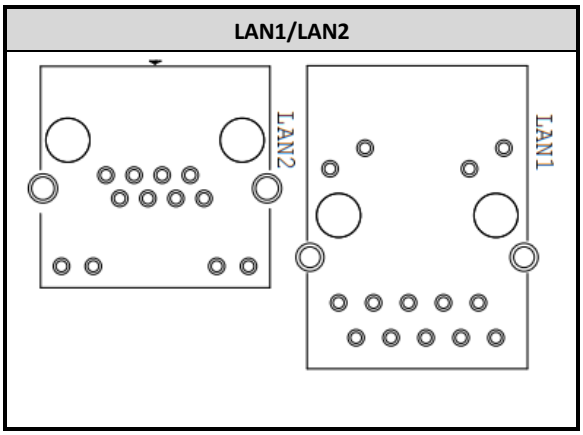
Signal	Pin		Signal
VCC 5V	1	2	VCC 5V
USB DATA-	3	4	USB DATA-
USB DATA+	5	6	USB DATA+
GND	7	8	GND
NC	9	10	(null)

2.12 LAN （labeled LAN1/LAN2 onboard）

The motherboard provides two RJ45 Ethernet ports:

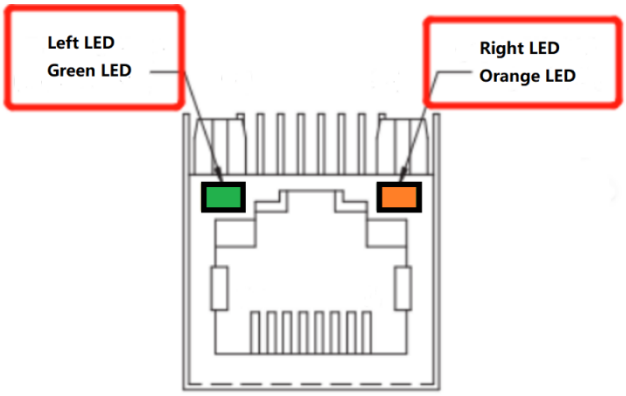
- LAN1: Intel i219-V controller, supporting speeds up to 1 Gbps
- LAN2: Intel i226-V controller, supporting speeds up to 2.5 Gbps
    - *Note: The Intel i226-V supports one-time MAC address programming only and cannot be reprogrammed.*

Both LAN1 and LAN2 support Wake-on-LAN (Magic Packet wake-up). LAN2 additionally supports UEFI PXE network booting. When using UEFI PXE boot, set IPv4 PXE Support = Enabled in the BIOS.



LED Status Indicators:

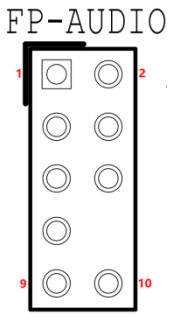
LI_LED (Green)	Function	ACT_LED (Orange)	Function
Always on	Network connected	Blinking	Data transfer active



2.13 Audio (labeled FP-AUDIO onboard)

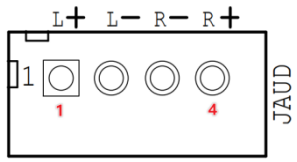
The motherboard integrates the Realtek ALC897 audio codec and provides rear-panel audio jacks (green: Line_out, pink: MIC_in). A front audio header labeled FP_AUDIO (2.54 mm pitch) is also provided, with the JAUD header supplying dedicated amplifier output signals.

Front Audio Header Pin Definition: Labeled FP-AUDIO onboard (2.54 mm)



Signal	Pin		Signal
MIC2-L	1	2	AGND
MIC2-R	3	4	AVCC (NC)
FRO-R	5	6	MIC2-JD
F-IO-SEN(AGND)	7	8	(null)
FRO-L	9	10	LIN2-JD

JAUD Amplifier Output Header: Labeled JAUD onboard (2.0mm)

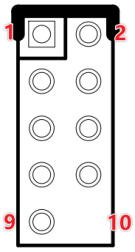


Pin	Signal
1	L+
2	L-
3	R-
4	R+

2.14 Serial Ports (Labeled JCOM1, JCOM2, COM36 onboard)

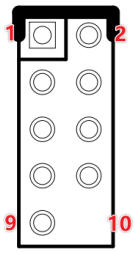
The motherboard provides six serial ports, all supporting RS-232 by default. COM1 and COM2 use 2.54 mm pin headers, while COM3–COM6 use 2.0 mm pin headers. COM1 can be configured for RS-485 operation through designated hardware modification.

COM1 Pin Definition: Labeled JCOM1 onboard (2.54 mm)



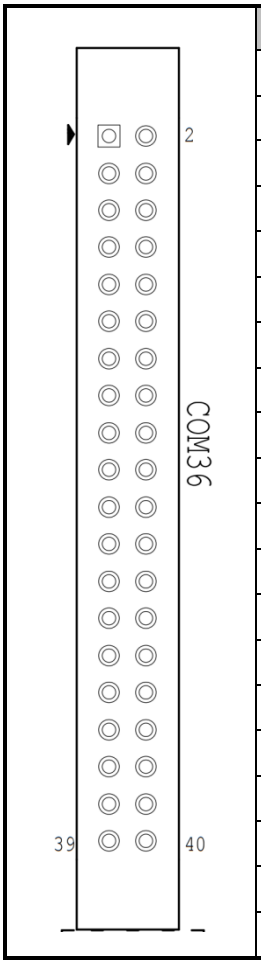
Pin	RS232	RS485
1	DCD#	DATA-
2	RXD	DATA+
3	TXD	(NC)
4	DTR#	(NC)
5	GND	GND
6	DSR#	(NC)
7	RTS#	(NC)
8	CTS#	(NC)
9	RI#	(NC)

COM2 Pin Definition: Labeled JCOM2 onboard (2.54 mm)



Signal	Pin		Signal
DCD#	1	2	RXD
TXD	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS#
RI#	9		

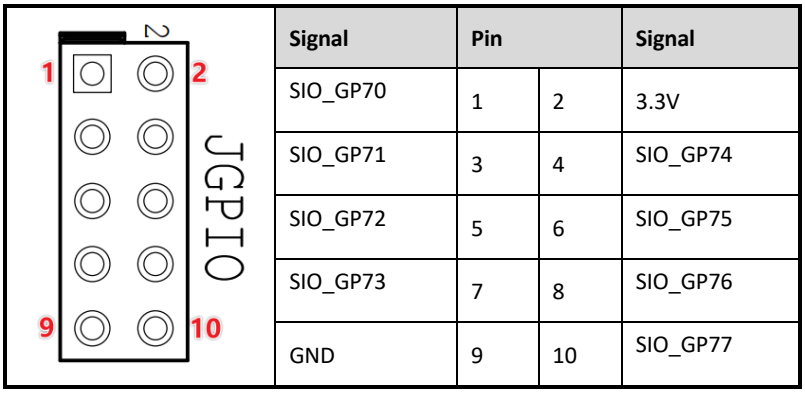
COM3-6 Pin Definition: Labeled COM36 onboard (2.0 mm)



Signal	Pin		Signal
DCD#	1	2	RXD
TXD	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS#
RI#	9	10	(NC)
DCD#	11	12	RXD
TXD	13	14	DTR#
GND	15	16	DSR#
RTS#	17	18	CTS#
RI#	19	20	(NC)
DCD#	21	22	RXD
TXD	23	24	DTR#
GND	25	26	DSR#
RTS#	27	28	CTS#
RI#	29	30	(NC)
DCD#	31	32	RXD
TXD	33	34	DTR#
GND	35	36	DSR#
RTS#	37	38	CTS#
RI#	39	40	(NC)

2.15 GPIO（Labeled GPIO onboard）

The motherboard provides a 2×5-pin JGPIO header (**Labeled GPIO onboard, 2.0 mm pitch**), providing eight programmable GPIO ports. Please refer to the appendix for GPIO configuration details.

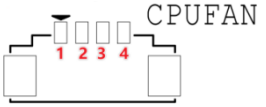


Signal	Pin		Signal
SIO_GP70	1	2	3.3V
SIO_GP71	3	4	SIO_GP74
SIO_GP72	5	6	SIO_GP75
SIO_GP73	7	8	SIO_GP76
GND	9	10	SIO_GP77

2.16 CPU Fan/ System Fan Socket（Labeled CPU_FAN, SYS_FAN onboard）

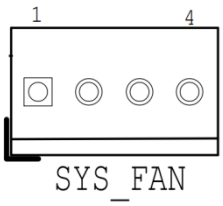
- 1 × CPU fan header (4-pin, 5V/12V; Labeled CPU_FAN onboard, 1.25 mm). A standard 5V heatsink is included by default.
- 1 × system fan header (4-pin, 5V/12V; Labeled SYS_FAN onboard, 2.54 mm).
- 1 × fan voltage selection header (5V/12V; Labeled JVCCFAN onboard, 2.0 mm).

CPU Fan Definition (Labeled CPU-FAN onboard)



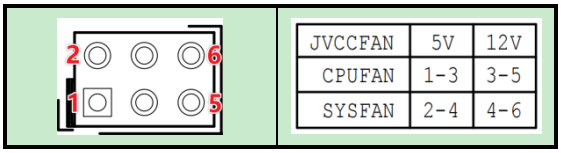
Pin	1	2	3	4
Signal	VCC	GND	TAC	CTL

System Fan Definition (Labeled SYS-FAN onboard)



Pin	1	2	3	4
Signal	GND	VCC	TAC	CTL

JVCCFAN Voltage Adjustment Pin (5V/12V; Labeled JVCCFAN onboard)

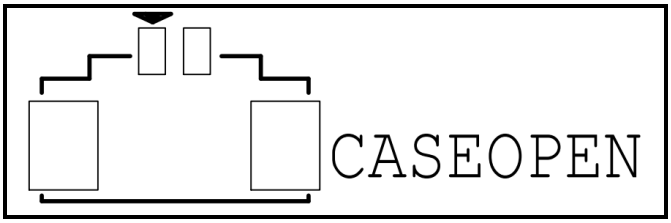


2.17 CASEOPEN Detection Pin (Labeled CASEOPEN onboard)

The CASEOPEN header is used for chassis-intrusion detection. When the chassis cover' switch is connected to this header, the system can determine whether the chassis has been opened and trigger the corresponding monitoring or protection functions.

This interface allows software or firmware to read intrusion status from the Super I/O registers. When the chassis cover is opened and the signal is interrupted, the Super I/O records the event, which can then be viewed through supported software or BIOS menus.

Pin Header: 1.25 mm (plug-and-play) See the diagram below.



Chapter 3 BIOS Setup

3.1 Entering the BIOS

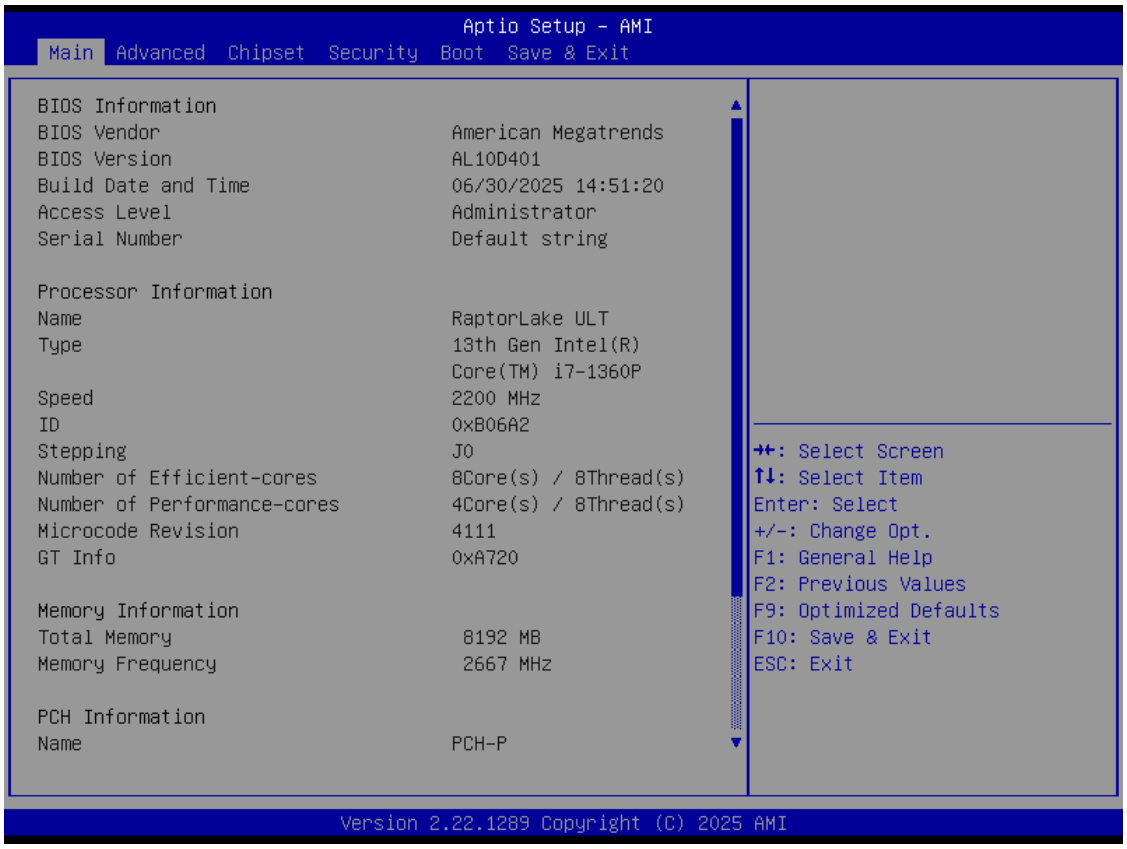
1. Turn on the computer and press <Delete> entering the BIOS
2. BIOS Hotkey Functions

BIOS Hotkey Functions:

Key	Function	Description
→ ←	Select Screen	Navigate between menu screens.
↑↓	Select Item	Move between menu items or options.
Enter	Select	Open a submenu or confirm a selection.
+/-	Change Option	Adjust values or change settings.
F1	General Help	Displays helpful information for the selected item.
F2	Previous Values	Load the previously saved settings.
F9	Optimized Defaults	Restore factory default settings.
F10	Save & Exit	Save changes and exit BIOS.
ESC	Exit	Exit BIOS or return to the previous menu.

3.2 Main Menu （BIOS Info, Date, Time）

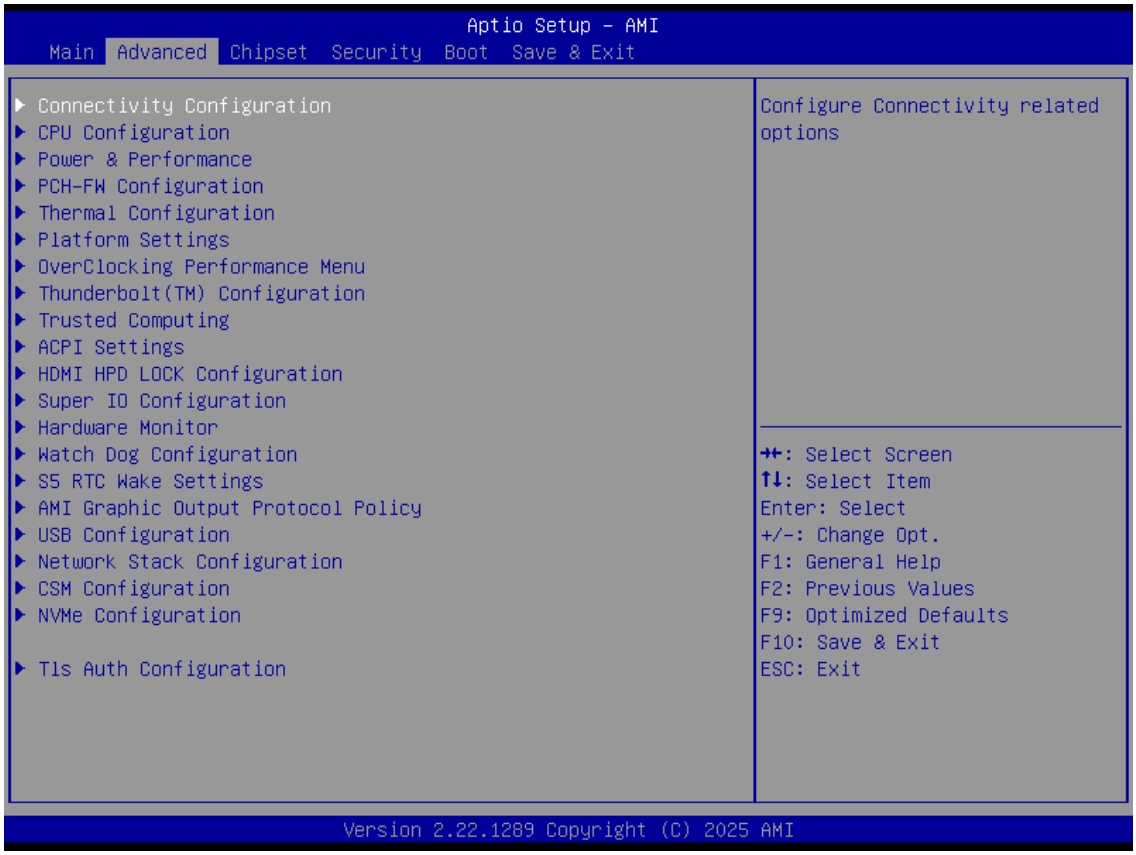
When you enter the BIOS Setup utility the first things you will encounter is the Main Setup screen. Shown below is the Main BIOS Setup screen. You can always return to the Main setup by selecting the Main tab.



BIOS Information

- BIOS Vendor: American Megatrends
- BIOS Version: Displays the current BIOS version
- Build Date and Time: BIOS build timestamp
- Processor Information: CPU identification details
- Total Memory: Installed system memory
- Memory Frequency: Active memory operating frequency
- PCH Information: Platform Controller Hub details
- PCH SKU: PCH model identifier
- ME FW Version: Intel Management Engine firmware version
- System Date: System date setting (format: MM/DD/YYYY)
- System Time: System time setting (format: HH:MM:SS)

3.3 Advanced Settings

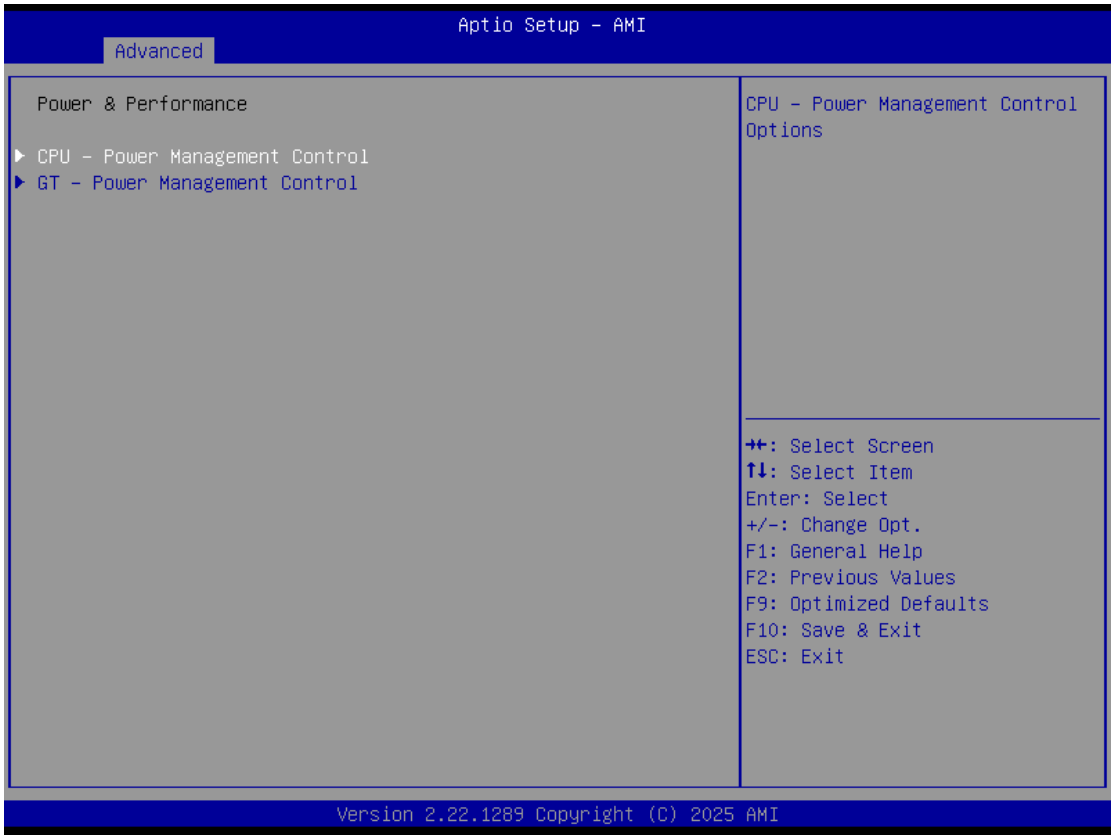


Selecting any item in the left pane opens its corresponding Advanced submenu. The Advanced section allows you to configure system features, adjust platform behavior, and modify CPU-related settings.

1. Connectivity Configuration: Connection Configuration
2. CPU Configuration: CPU Parameter Information and Common Settings Selection
3. Power & Configuration: Power & Configuration
4. PCH-FW Configuration: PCH Firmware Configuration
5. Thermal Configuration: Thermal Configuration
6. Platform Settings: Platform configuration options
7. OverClocking Performance Menu: Overclocking settings
8. Thunderbolt™ Configuration: Thunderbolt interface configuration
9. Trusted Computing: TPM and trusted computing settings
10. ACPI Settings: ACPI power state configuration
11. HDMI HPD Lock Configuration: HDMI hot-plug detect lock settings
12. Super IO Configuration: Super IO Configuration
13. Hardware Monitor: System voltage, temperature, and fan monitoring
14. Watch Dog Configuration: Watchdog timer configuration
15. S5 RTC Wake Settings: RTC wake-up configuration for S5 state
16. AMI Graphic Output Protocol Policy: Graphics output (GOP) policy settings
17. USB Configuration: USB Configuration
18. Network Stack Configuration: Network Stack Configuration
19. CSM Configuration: Compatibility Support Module settings

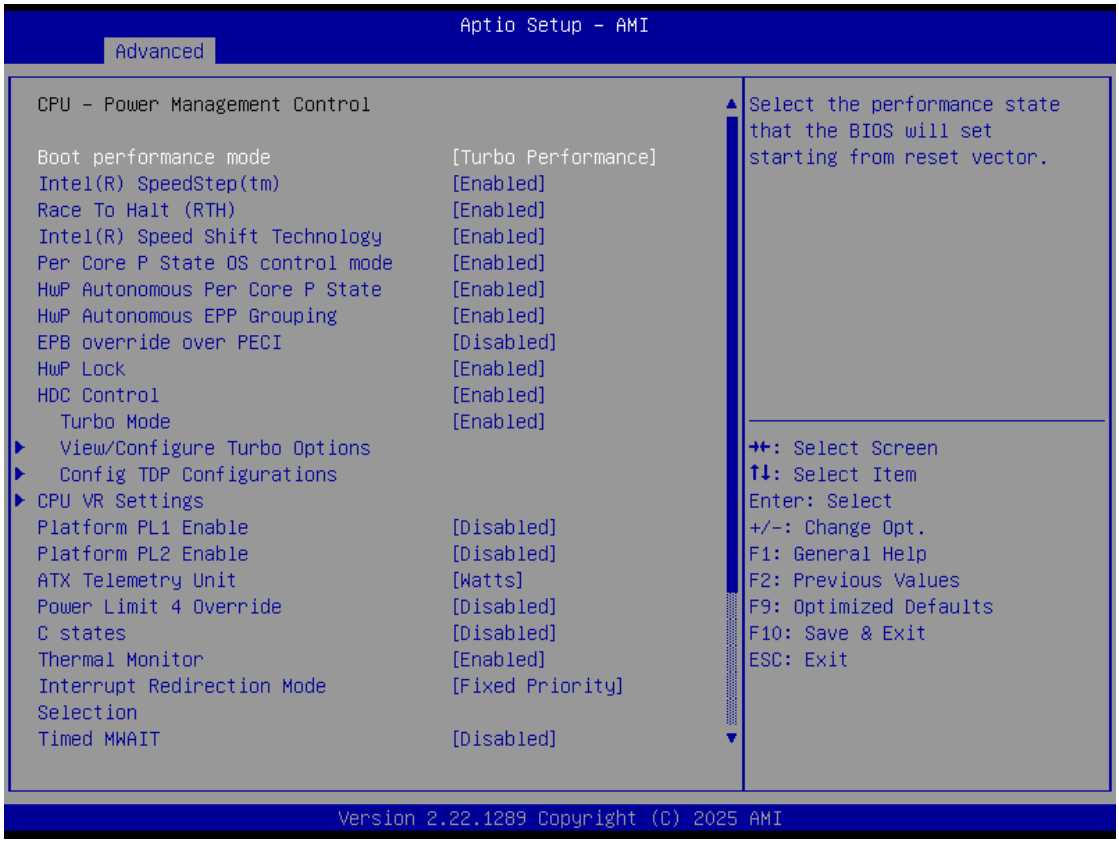
20. NVMe Configuration: NVMe Storage Device Configuration
21. TLS Auth Configuration: TLS Authentication Configuration

3.3.1 Power & Configuration



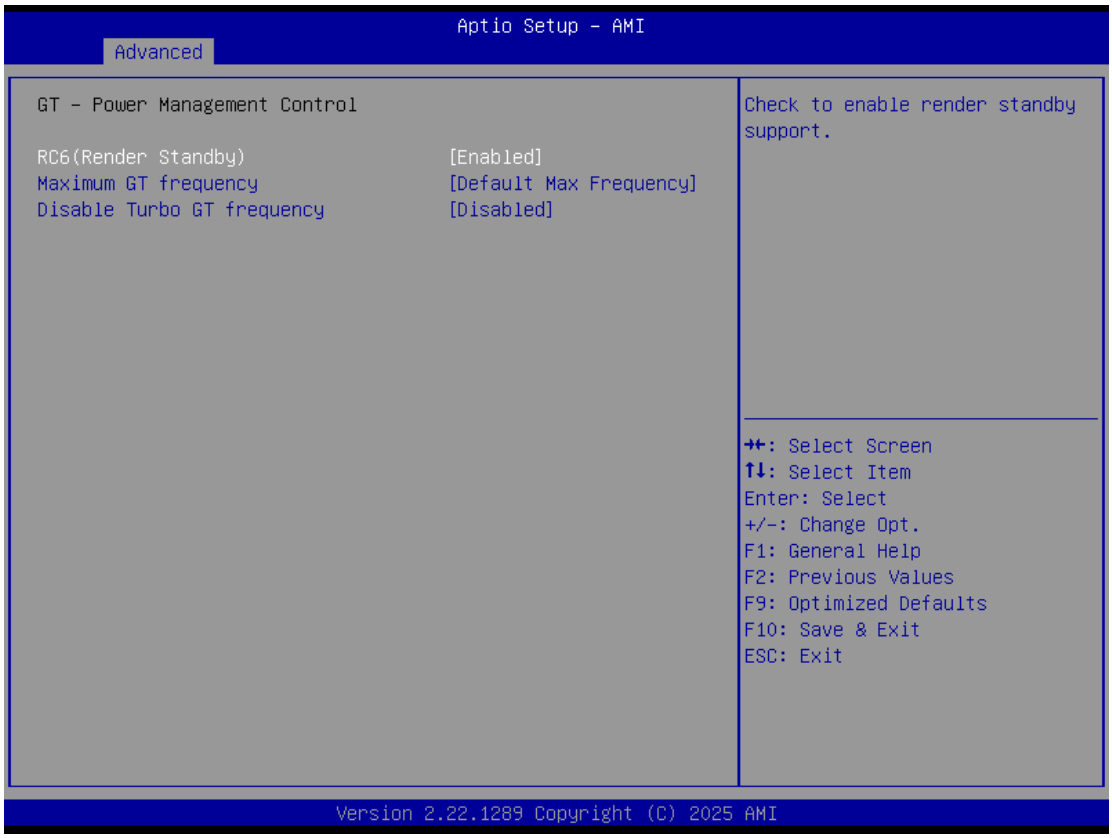
1. CPU-Power Management Control
2. GT-Power Management Control

3.3.2 CPU-Power Management Control



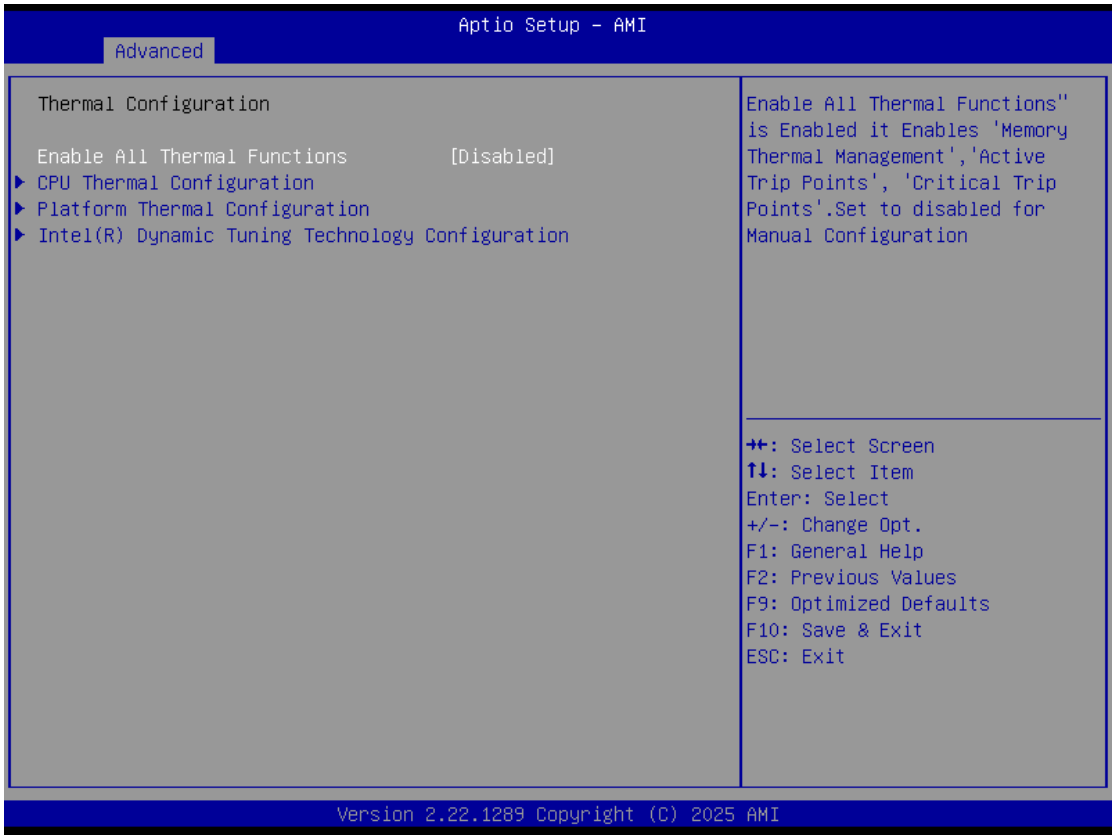
- **Boot Performance Mode:** Determines the initial CPU performance state during boot. Options include Default Turbo Performance, Max Battery, and Max Non-Turbo Performance.
- **Intel® SpeedStep™ Technology:** Enables dynamic adjustment of CPU voltage and frequency based on workload to reduce power consumption and thermal output.
- **Intel® Speed Shift Technology:** Provides hardware-controlled, faster voltage/frequency transitions for improved responsiveness and efficiency. Default: Enabled
- **Per-Core P-State OS Control Mode**: Allows the operating system to control individual per-core performance states.
- **HwP Autonomous Per-Core P-State:** Enables autonomous hardware-managed per-core performance state control.
- **HwP Autonomous EPP Grouping:** Enables autonomous grouping of Energy Performance Preference (EPP) settings.
- **EPB Override Over PCIe:** Allows the system to override Energy Performance Bias via PCIe.
- **Platform PL1 Enable:** Controls Platform Power Limit 1. Default: Disabled
- **Platform PL2 Enable:** Controls Platform Power Limit 2. Default: Disabled
- **Power Limit 4 Override:** Enables override of Power Limit 4. Default: Disabled
- **C States:** Controls CPU idle power states. C0 represents full activity; deeper C-states (C1–C6) progressively reduce clocks and voltage to save power at the cost of wake latency. Default: Enabled
- **Enhanced C States:** Enables enhanced idle-state power optimization, combining clock gating (C1–C3) and voltage reduction (C4–C6). Default: Enabled

3.3.3 GT-Power Management Control



1. **RC6(Render Standby):** (Standby)Enable/disable integrated graphics standby, default Enabled.
2. **Maximum GT frequency:** Maximum GT Frequency, Default max frequency.
3. **Disable Turbo GT frequency**: Disable Turbo GT Frequency mode, Default disabled.

3.3.4 Thermal Configuration



Enable All Thermal Functions

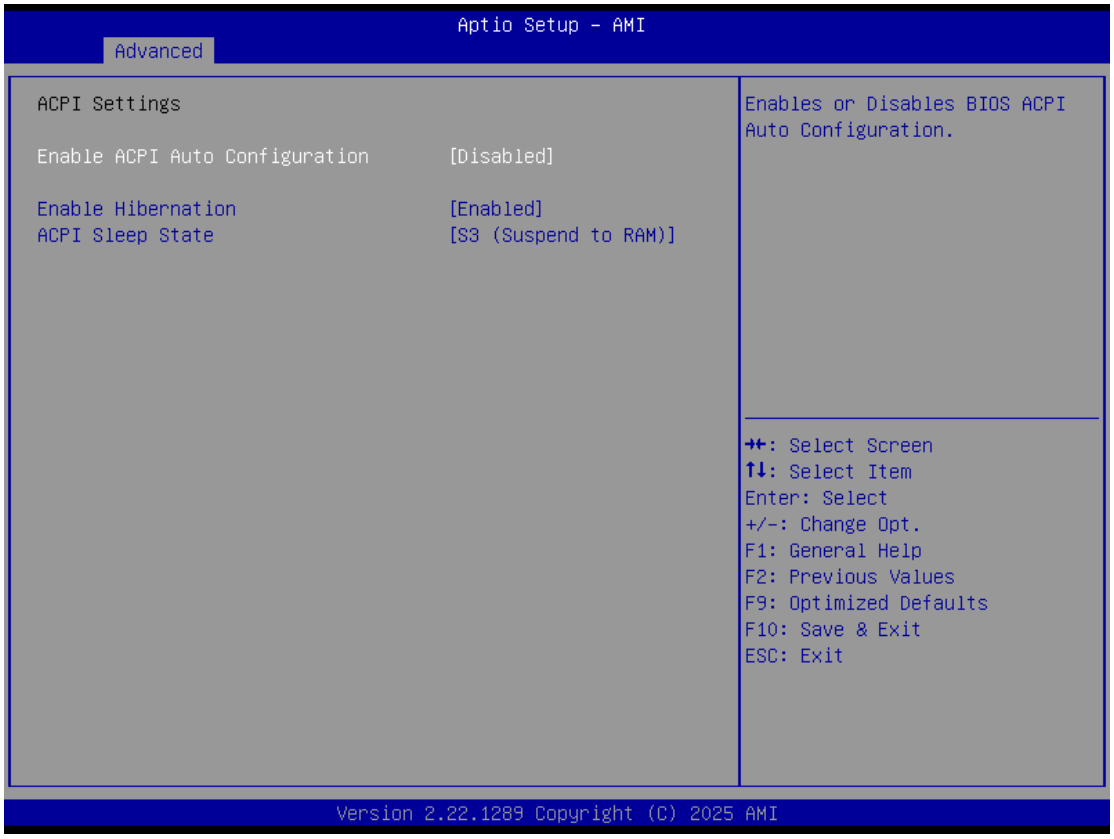
CPU Thermal Configuration:

Unlocks the temperature setting, the “Tcc Activation Offset” is the temperature adjustment option, the highest temperature is 100°C. Change the temperature by minus the number of degrees you wish to change. For example, minus 0(100-0) to set the temperature at 100°C, minus 20(100-20) to set the temperature at 80°C. (Please note the maximum supported temperature for the processor can be found on ark.intel.com.)

Platform Thermal Configuration

Intel(R) Dynamic Tuning Technology Configuration

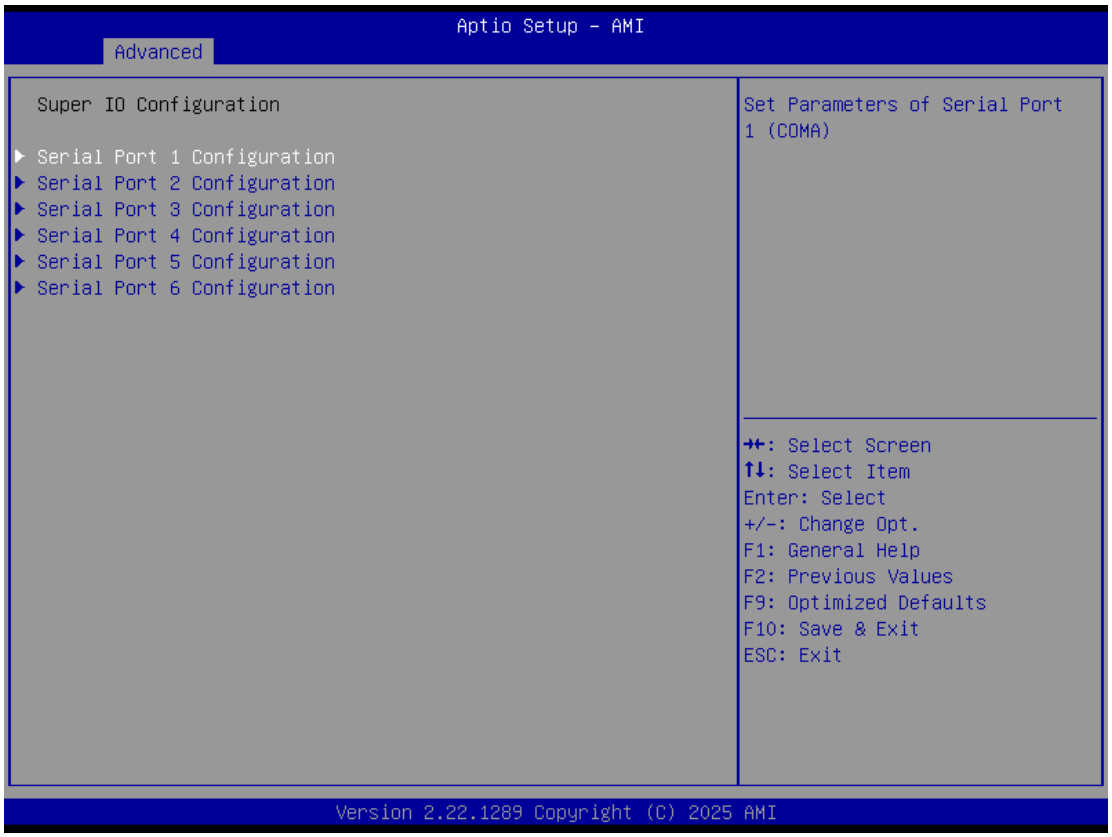
3.3.5 ACPI Settings



ACPI Settings

- Enabled ACPI Auto Configuration
- Enabled Hibernation
- ACPI Sleep State

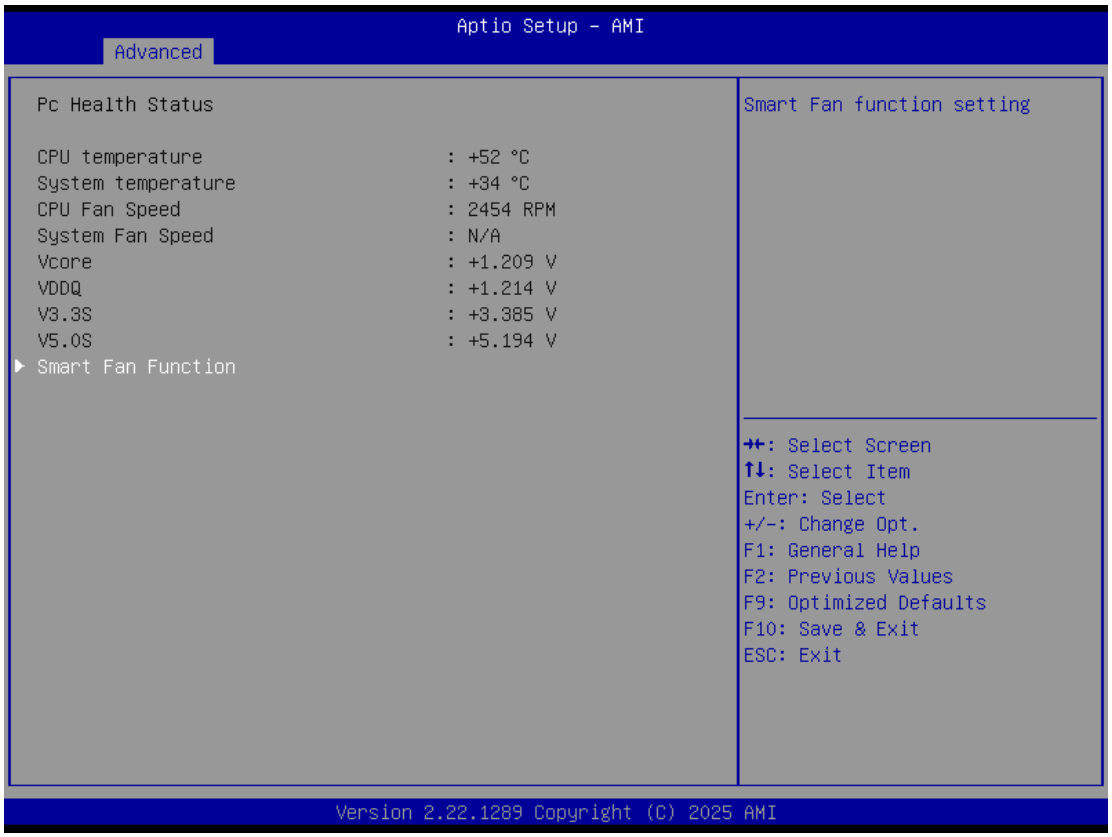
3.3.6 Super IO Configuration



Serial Port 1~6 Configuration

- **Serial Port:** Enable or disable serial port (COM).
- **Device Setting (Read-only):** Displays serial ports' interrupt and location.
- **Change Setting:** Change serial port settings and **default setting is recommended as "Auto".**

3.3.7 Hardware Monitor

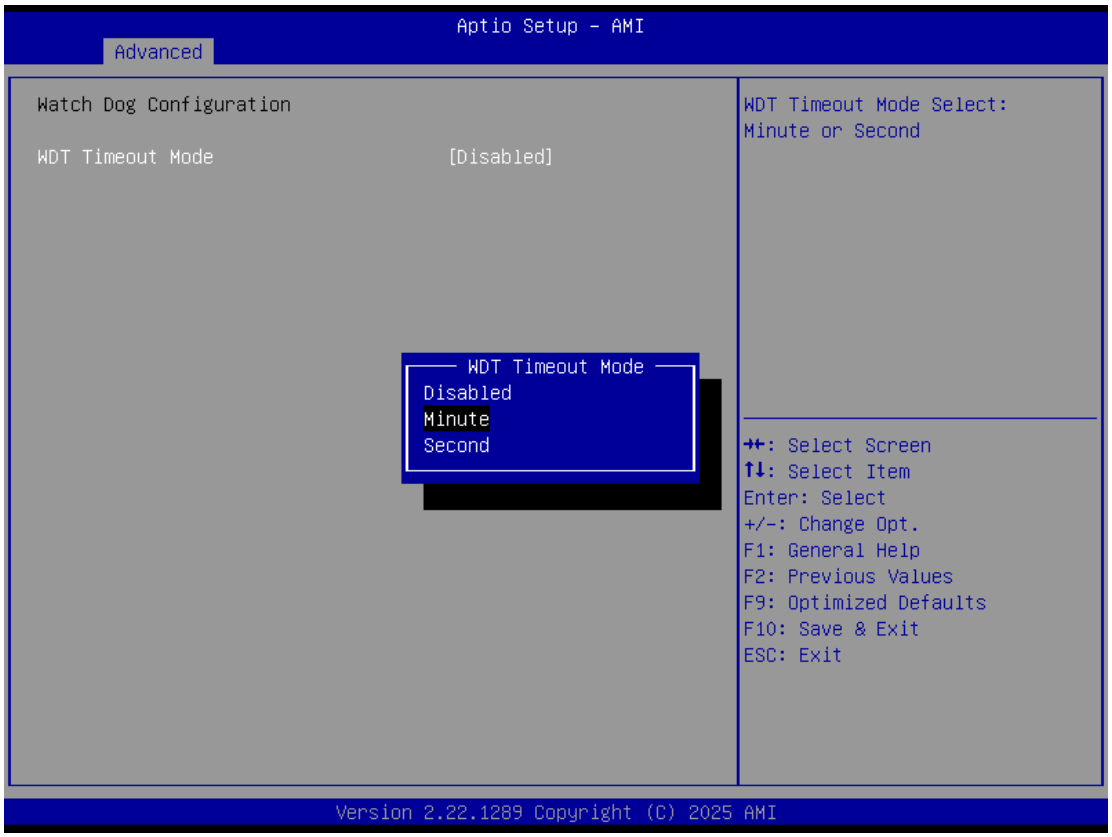


PC Health Status

The PC health status displays CPU temperature, system temperature, fan speed, and other relevant voltage values. The above parameters have a certain range, and the system cannot run beyond these ranges.

1. CPU Temperature
2. System Temperature
3. CPU Fan Speed
4. System Fan Speed
5. VCore: +1.100V (CPU core voltage)
6. VDDQ: +1.225V (RAM voltage)
7. V3.3S
8. V5.0S
9. Smart Fan Funtion
    - System Smart Fan Mode
    - CPU Smart Fan Mode
    - Automatic Mode
    - Full on Mode
    - Manual Mode

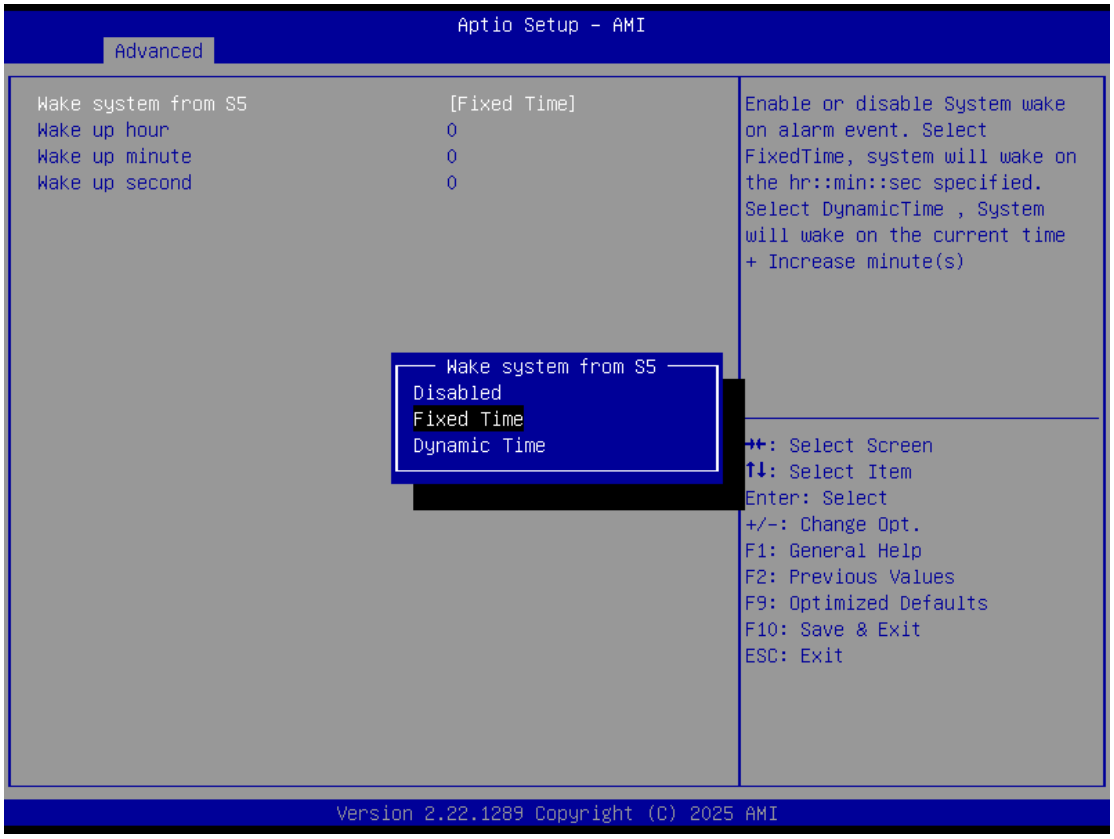
3.3.9 Watch Dog Configuration



Watch Dog Configuration

- WDT Timeout Mode select: Minute or Second

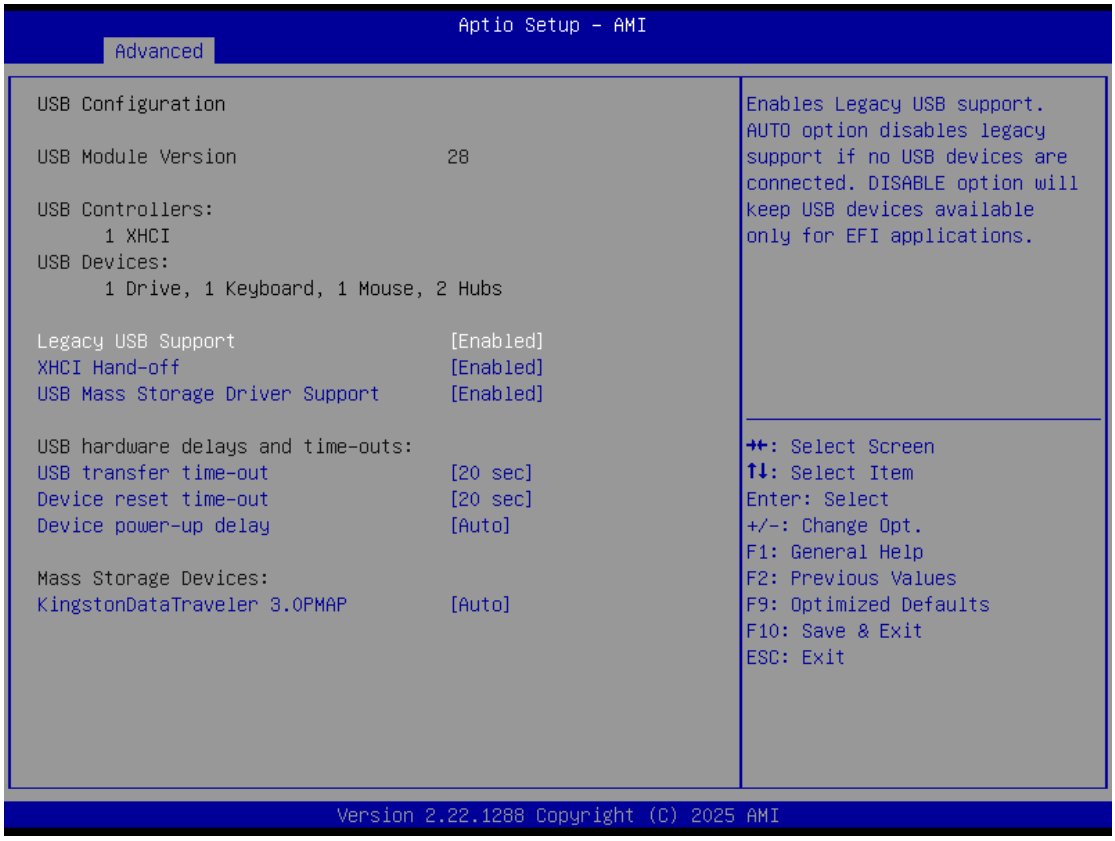
3.3.10 S5 RTC Wake Settings



Wake system From S5: Allows the system to power on automatically from an S5 state. Disabled by default.

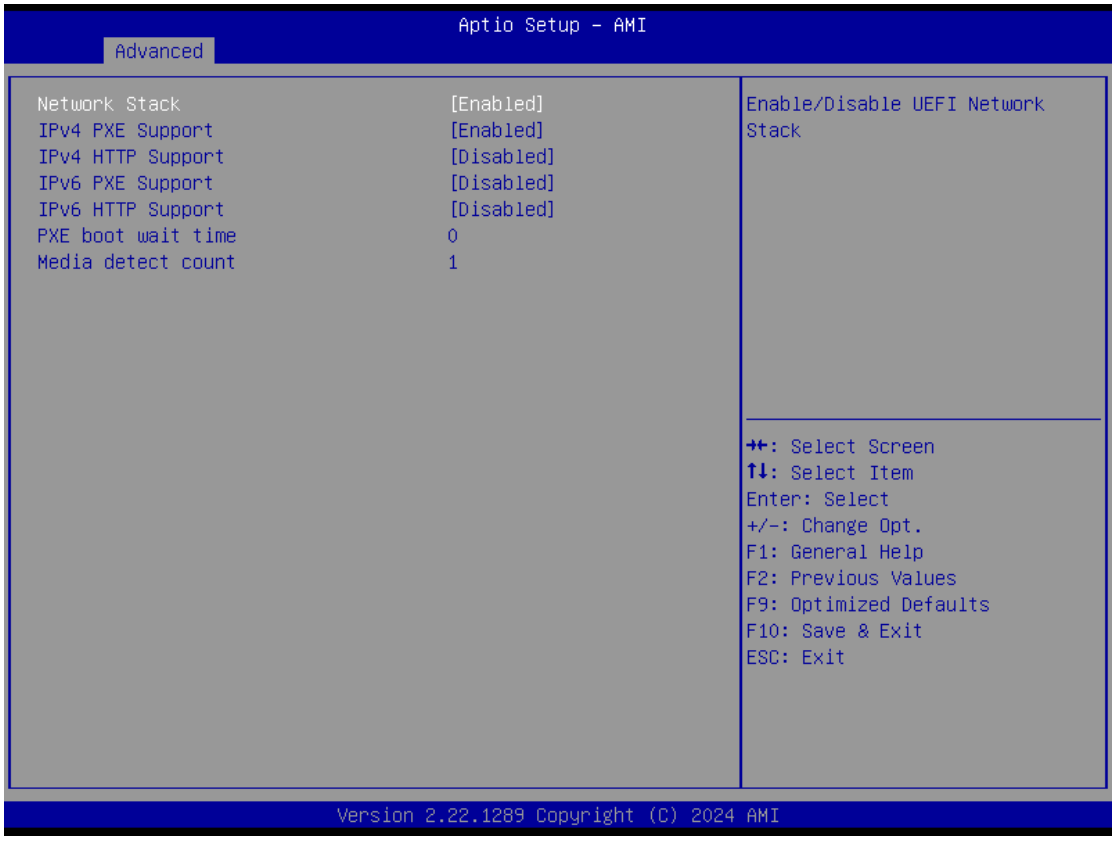
- **Fixed Time:** Select Fixed Time and the system will wake on the Hr: Min: Sec specified.
- **Dynamic Time:** Select Dynamic Time and the system will wake on a dynamic time.

3.3.11 USB Configuration



1. **Legacy USB Support**
   a) Enable Legacy USB support. Disables legacy support if no USB devices are connected. Select enable will keep USB devices available under UEFI's support.
2. **XHCI Hand-off**
   a) A workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the USB XCHI driver.
3. **USB Mass Storage Driver Support**
   a) Enable(default) or disable USB Mass Storage Driver Support.
4. **USB transfer time-out**
   a) Sets the timeout for control, bulk, and interrupt transfers, default: 20 second.
5. **Device reset time-out**
   a) Defines the timeout for USB mass storage device start-up, default: 20 second.
6. **Device Power-up Delay**
   a) Specifies the maximum time a USB device may take to report itself to the host controller.

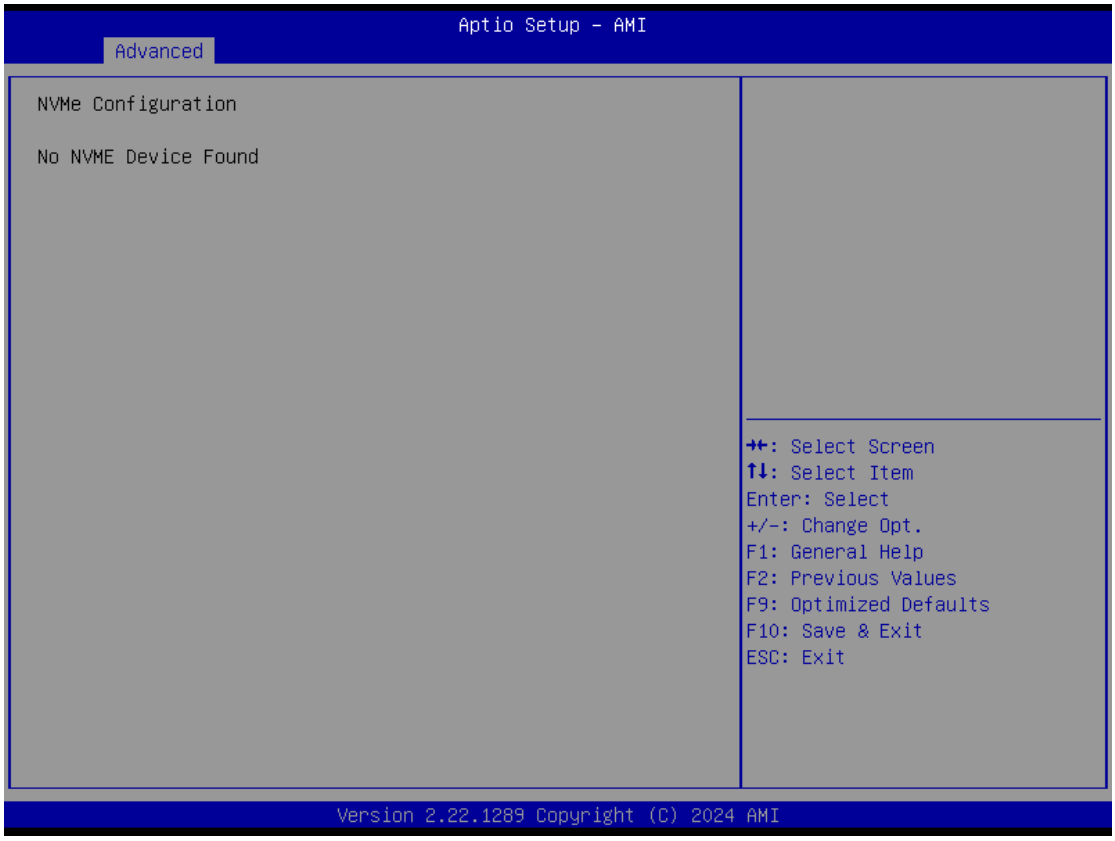
3.3.12 Network Stack Configuration



Network Stack : PXE Network boot setting, disabled by default.

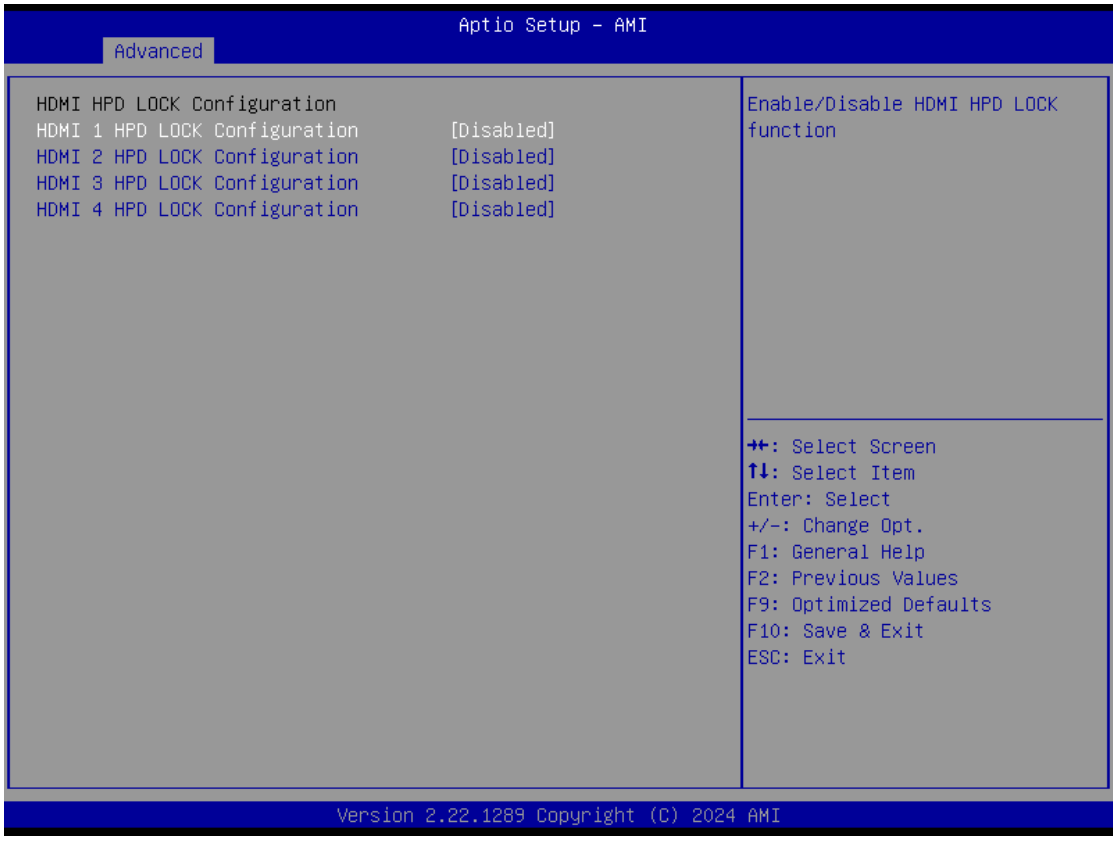
- IPv4 PXE Support
- IPv4 HTTP Support
- IPv6 PXE Support
- IPv6 HTTP Support
- PXE boot wait time
- Media detect count

3.3.13 NVME Configuration



The capacity and model of the SSD will be displayed under the option after the NVMe protocol SSD has been installed.

3.3.14 HDMI HPD LOCK Configuration



Controls Hot-Plug Detect (HPD) lock behavior for each HDMI port. When Enabled, the HDMI display connection is locked; when Disabled, normal HPD behavior is used.

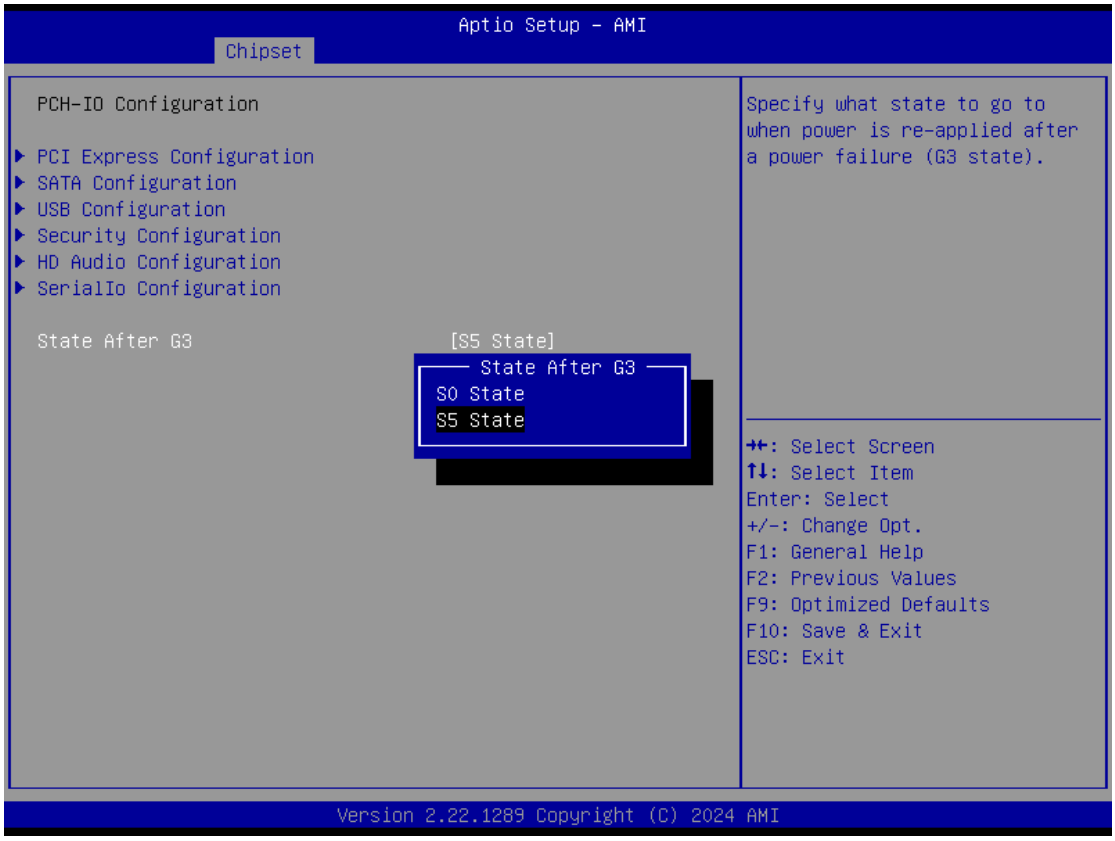
- HDMI 1 HPD LOCK Configuration – Enable/Disable HPD lock
- HDMI 2 HPD LOCK Configuration – Enable/Disable HPD lock
- HDMI 3 HPD LOCK Configuration – Enable/Disable HPD lock
- HDMI 4 HPD LOCK Configuration – Enable/Disable HPD lock

3.4 Chipset

System Agent (SA) Configuration: Northbridge configuration options, including video memory, display devices, and other options.

PCH-IO Configuration: Southbridge configuration options, including hard disk, sound card equipment, and other options

3.4.1 State After G3

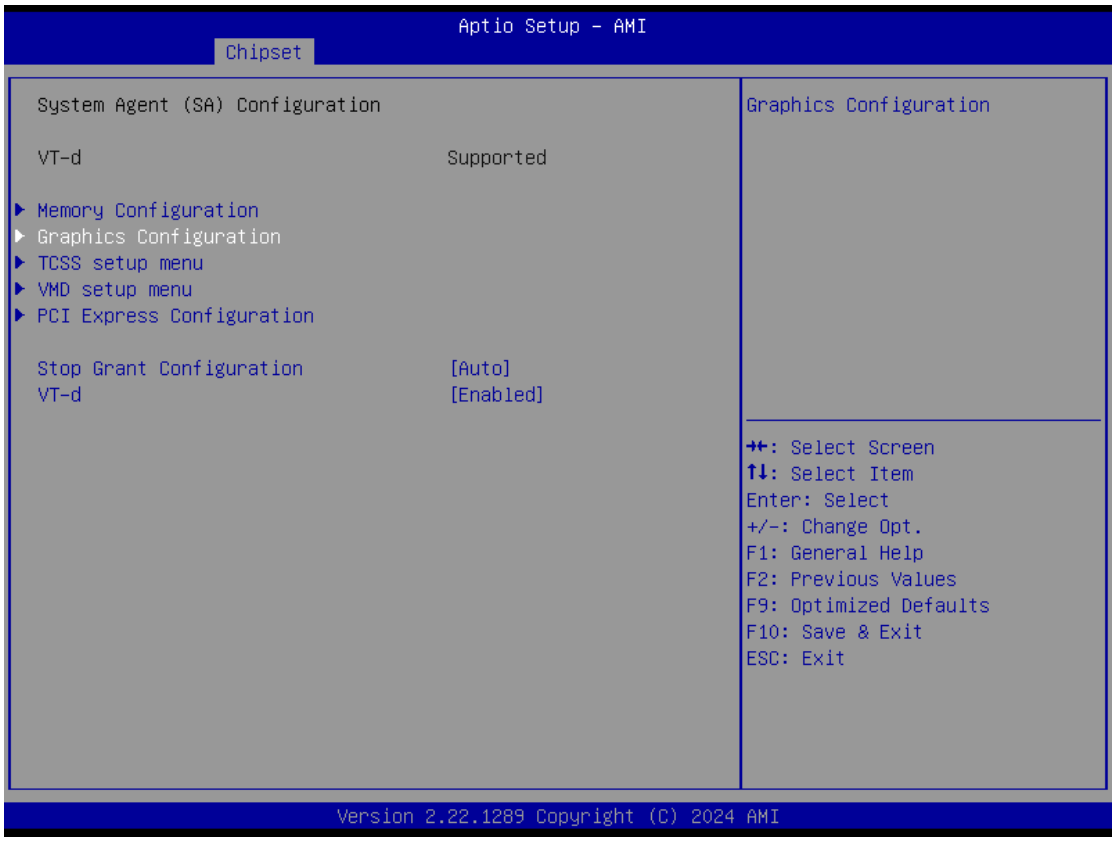


1. **PCI Express Configuration**
2. **SATA Configuration**
3. **USB Configuration**
4. **Security Configuration**
5. **HD Audio Configuration**
6. **Serial IO Configuration**
7. **State After G3:**
    i. S0 State (system power-on, self-start)
    ii. S5 State (system power-on, shutdown). Set by default.

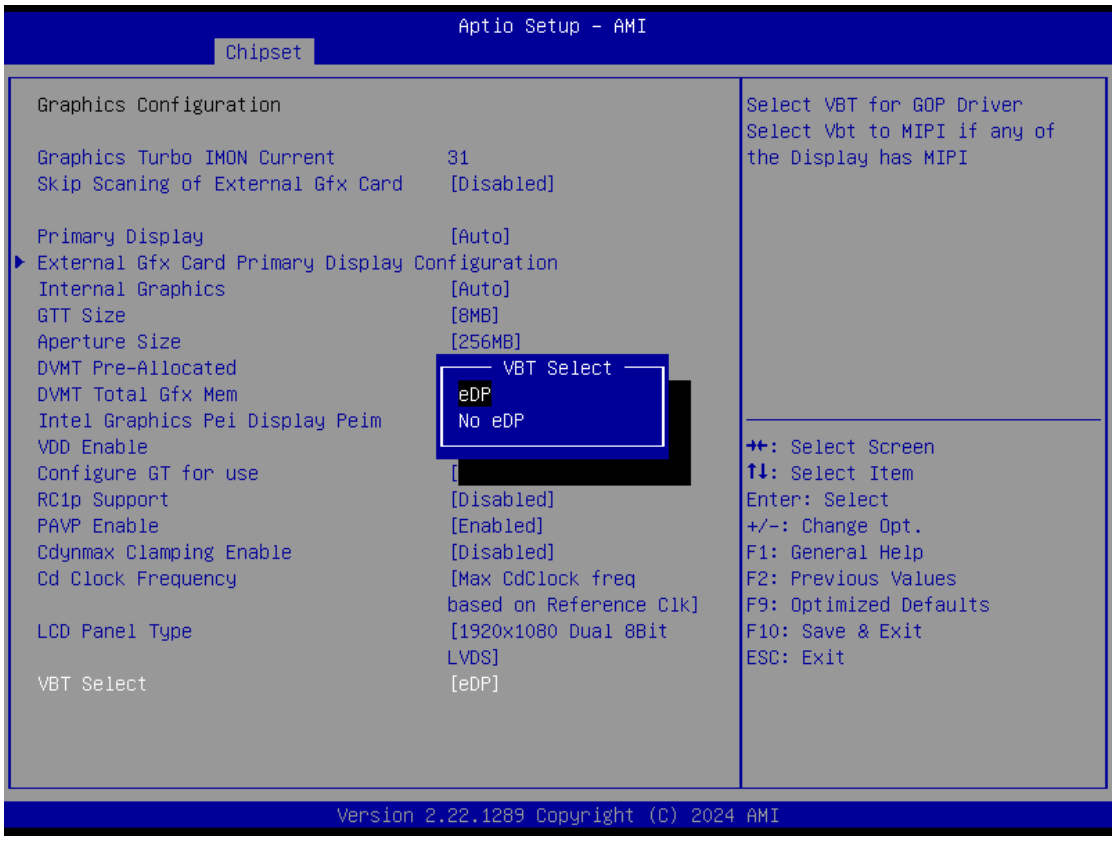
3.4.2 Steps to Configure LVDS in BIOS

1. Press the DEL key to enter the bios interface, use the left and right arrow keys on the keyboard to get the Chipset section, select "System Agent (SA) Configuration" to enter, as shown below:

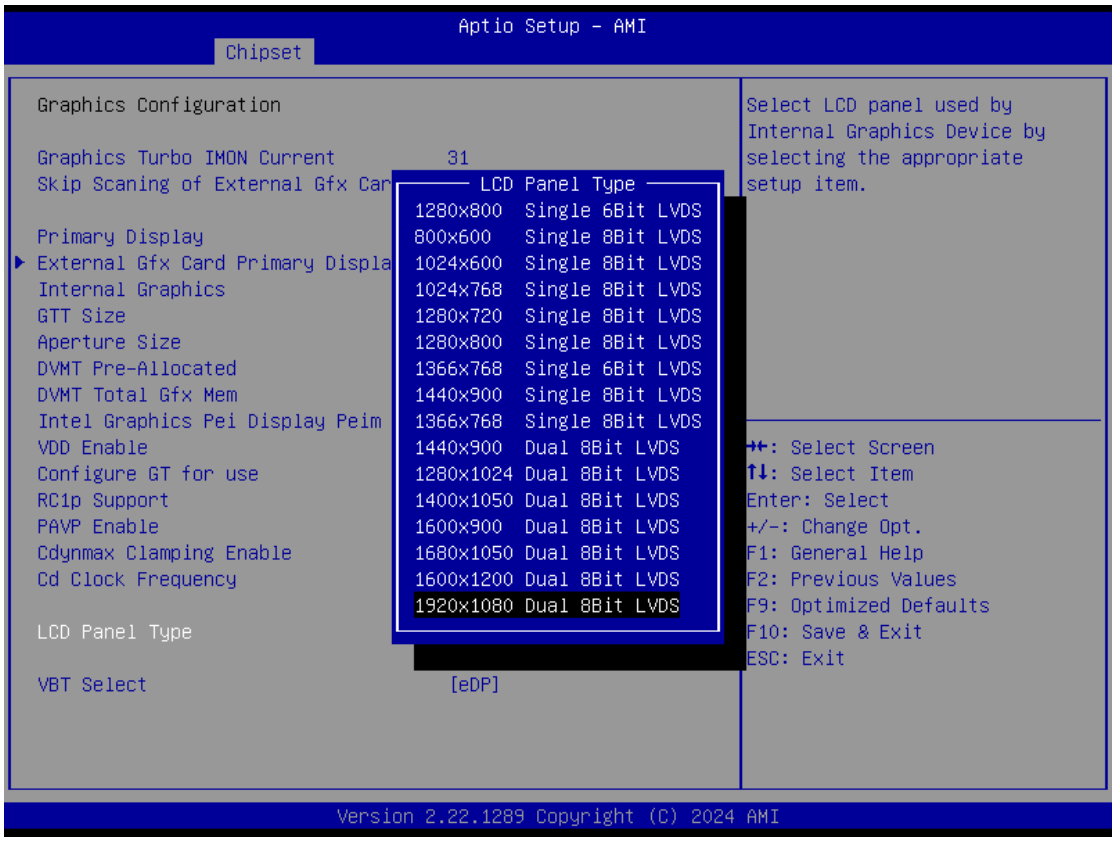
2. Select "Graphics Configuration" then press enter, as shown below:



3. Select the "VBT Select" option to turn the LVDS ON or OFF (LVDS OFF: No eDP, LVDS ON: eDP) as shown below:



4. Select "LCD Pane Type" press enter, then select the target resolution (each monitor's tech specification has the screen-supported resolution), 5After selecting the target screen resolution, press F10 to save and exit. Reference as shown below:



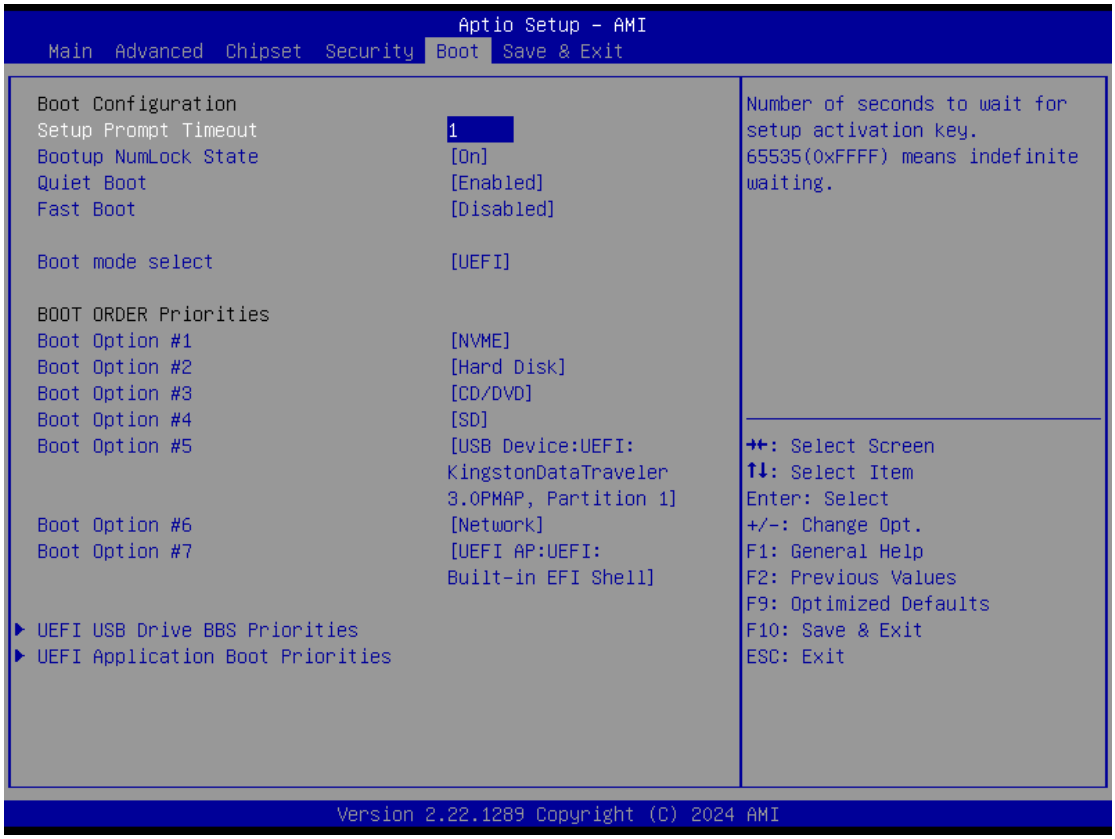
3.5 Security

Administrator Password: Set the Administrator Password.

User Password: Set User Password.

Secure Boot: Secure boot

3.6 BOOT



Setup Prompt Timeout:

Number of seconds that the firmware will wait before initiating the original default boot selection. A value of 0 indicates that the default boot selection is to be initiated immediately on boot. A value of 65535(0xFFFF) indicates that firmware will wait for user input before booting. This means the default boot selection is not automatically started by the firmware.

Bootup NumLock State:

Select the keyboard NumLock state

Quiet Boot: Enable this option to display the full logo; disable it to show only a text prompt (default Enabled is on, Disabled is off)

Fast Boot: Enable this option for quick startup (Disabled is off, Enabled is on)

Boot Mode Select: Select Boot Mode

Boot Option #1~#7:

Set the system boot order from Number 1 to Number 7.

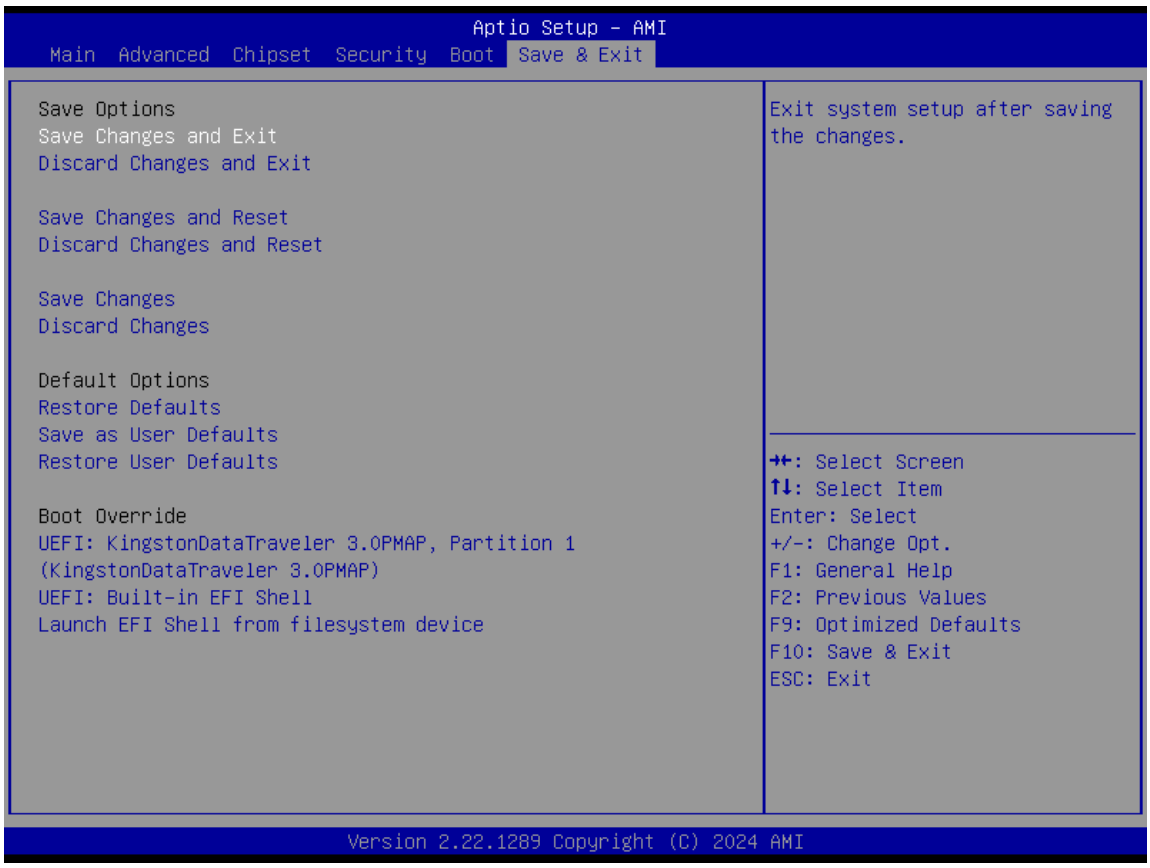
UEFI USB Drive BBS Priorities:

UEFI USB Drive BBS priorities setting.

UEFI Application boot Priorities:

UEFI application boot priority.

3.7 Save & Exit



Save Changes and Exit: Exit the system setup after saving the changes and continue to start the computer.

Discard Changes and Exit: Exit the system setup without saving any changes and continue to start the computer.

Save Changes and Reset: Reset the system after saving the changes.

Discard changes and Reset: Reset the system without saving any changes.

Save Changes: Save changes done so far to any of the options.

Discard Changes: Discard changes done so far to any of the options.

Restore Defaults: Restore/load default values for all the options.

Save as User Defaults: Save the changes done so far as the user defaults.

Restore User Defaults: Restore the user defaults to all the options.

Boot Override: Boot device selection can override your boot priority. Select the specified boot device such as SATA, USB Flash Disk, EFI Shell, PXE, etc., and boot directly. Or press F11 boot by selecting the specified boot device.

Pressing F11 during startup allows you to directly select a specific device to boot from.

Appendix

GPIO Setting

Accessing GPIO70:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x01); //Bit0=1 set as output，bit0=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x01); // When set as output, Bit0 of I/O address 0xA06 = 1 outputs high level, Bit0 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit0=1 Set as output，bit0=0 Set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); //When set as input, Bit0 of I/O address 0xA06 reflects the read state.

Accessing GPIO71:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x02); // Bit1=1 set as output， bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x02); // When set as output, Bit1 of I/O address 0xA06 = 1 outputs high level, Bit1 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); // Bit0=1 set as output， bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit1 of I/O address 0xA06 reflects the read state.

Accessing GPIO72:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x04);    //Bit2=1 set as output，bit2=0 set as input
WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x04); // When set as output, Bit2 of I/O address 0xA06 = 1 outputs high level, Bit2 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit2 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO73:

Example: Accessing via IO

Set as output：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x08); //Bit3=1 set as output，bit3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x08); // When set as output, Bit3 of I/O address 0xA06 = 1 outputs high level, Bit3 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit3=1 set as output，bi3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit3 of I/O address 0xA06 reflects the read state.

Accessing GPIO74:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x10);    //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x10); // When set as output, Bit4 of I/O address 0xA06 = 1 outputs high level, Bit4 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit4 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO75:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x20);    //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x20); // When set as output, Bit5 of I/O address 0xA06 = 1 outputs high level, Bit5 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit5 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO76:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x40);    //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x40); // When set as output, Bit6 of I/O address 0xA06 = 1 outputs high level, Bit6 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit6 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO77:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x80);    //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x80); // When set as output, Bit7 of I/O address 0xA06 = 1 outputs high level, Bit7 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit7 of I/O address 0xA06 reflects the read state.
```