User Manual

FP535 V1.0

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FP535 User Manual

(Version 1.0)

Release Notes:		
No.	Description	Date
V1.0	Initial Version	2025/11/10

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Warning

1. Before using the product, carefully read the manual to ensure proper installation and operation.
2. If you are not ready to install any extension card, store it in an anti-static protective bag to prevent damage.
3. To discharge any static electricity, briefly touch a grounded metal object before removing the extension card from the protective bag.
4. Always wear anti-static gloves and handle the card by its edges to avoid damaging sensitive components.
5. Verify that the power supply voltage is correct before connecting the motherboard to the power supply.
6. To prevent electric shock or damage, always turn off the AC power or unplug the power cord before removing or reconfiguring the motherboard or any components.
7. Unplug the AC power cord from the outlet before relocating the motherboard or any components.
8. Ensure all power cords are unplugged before connecting or disconnecting any equipment to avoid electrical hazards.
9. Wait at least 30 seconds after powering off the system before powering it on again to prevent unnecessary wear.
10. If any issues arise during operation, consult a qualified professional for assistance.
11. This product may cause radio interference in certain environments; if necessary, users should take appropriate measures to mitigate such interference.

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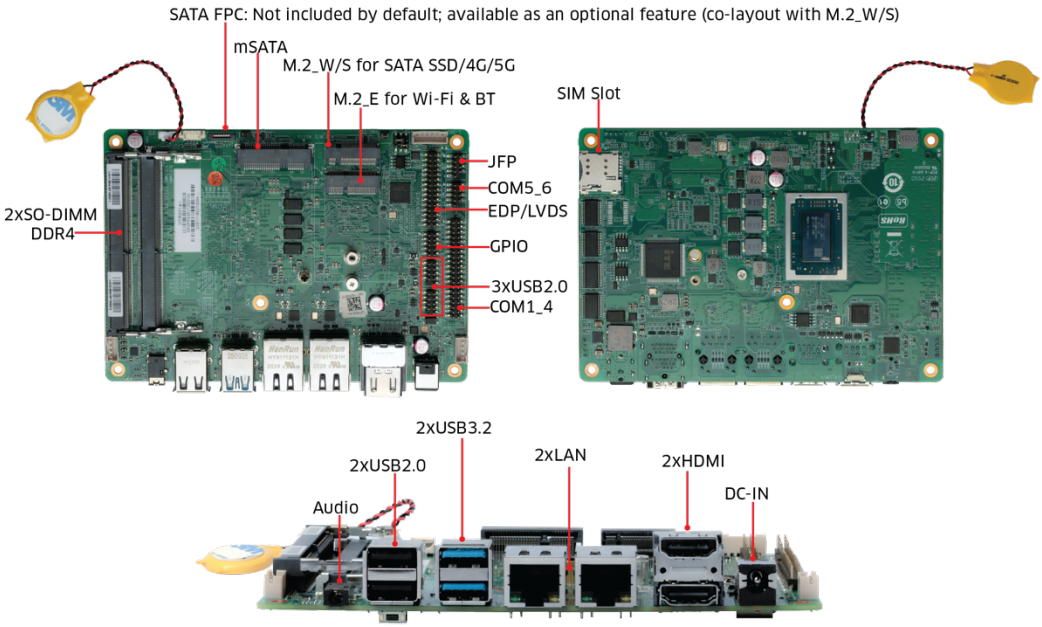
Chapter 1 Product Introduction

1.1 Brief Introduction

The FP535 is a 3.5" single board computer (SBC) based on the AMD Ryzen™ Embedded R2000 Series platform. It features a compact form factor combined with high performance computing, making it ideal for energy-efficient applications.



1.2 Parameters

CPU: AMD Ryzen™ Embedded R2000 Series

CPU	Cores/Threads	Base Freq.	Max Freq.	Total L3 Cache	Nominal TDP (cTDP Range)
R2312	2C/4T	2.7GHz	3.7GHz	4MB	15W (12-25W)
R2314	4C/4T	2.1GHz	3.5GHz	4MB	15W (12-35W)
R2514	4C/8T	2.1GHz	3.5GHz	4MB	15W (12-35W)

GPU: AMD Radeon™ Graphics

Display: Features 2xHDMI 2.0 ports and 1x LVDS port (optional eDP configuration, labeled as EDP/LVDS on board).

RAM: 2x SO-DIMM DDR4-2400/2667MHz, supports dual-channel, maximum capacity: 64GB

Storage/Expansion:

- 1 x mSATA for SSD (labeled as MSATA on board)
- 1 x M.2 Key E for 2230 Wi-Fi & BT Module (labeled as M.2_E on board, support PCIE/USB2.0)
- 1 x M.2 Key B for 2242 SATA SSD/3042 4G/ 3052 5G (labeled as M.2_W/S on board, When an SSD or 4G module is installed, the PWR-SSD jumper must be populated.)
- 1 x SATA3.0 FPC (labeled as SATA on board) co-layout with M.2 Key B Slot. Optional feature; Not included by default.

Audio: SenaryTech SN6186 High-Definition Audio Codec, support 1xCTIA Audio Jack, Line_out+Mic_in in one, supports power amplifier.

Ethernet: 2x Realtek RTL8111H Gigabyte Network Controllers. Date Rate Per Port: 1.0GbEs.

USB:

- 2 × USB 3.2 Gen 2 Type-A rear ports (10 Gbps; labeled as USB30 on board).
- 5 × USB 2.0 ports (480 Mbps), including:
    - 2 × USB 2.0 Type-A rear ports (labeled as USB20 on board).
    - 3 × USB 2.0 via onboard pin headers (2.0 mm pitch), with 2 ports routed from USB21 and 1 port routed from USB22.

Serial COM: 6 × COM headers (2.0 mm pitch), supporting 4 × RS-232 (COM1–COM4) and 2 × RS-485 (COM5–COM6) by default. COM5–COM6 can be optionally configured as RS-232 via hardware modification.

GPIO: 8-bit GPIO (labeled: GPIO, 2.0 mm)

TPM: External TPM module support (Infineon SLB9670, optional).

Other I/O:

- a set of JFP pins (labeled as JFP on board) (2.0mm)
- a set of JAT hardware auto-start pins (labeled as JAT on board) (2.0mm)
- a set of JAUD amplifier pins (labeled as JAUD on board) (2.0mm)
- a set of 5V 4-pin CPU fan pins (labeled as CPU_FAN on board)
- a SIM card slot

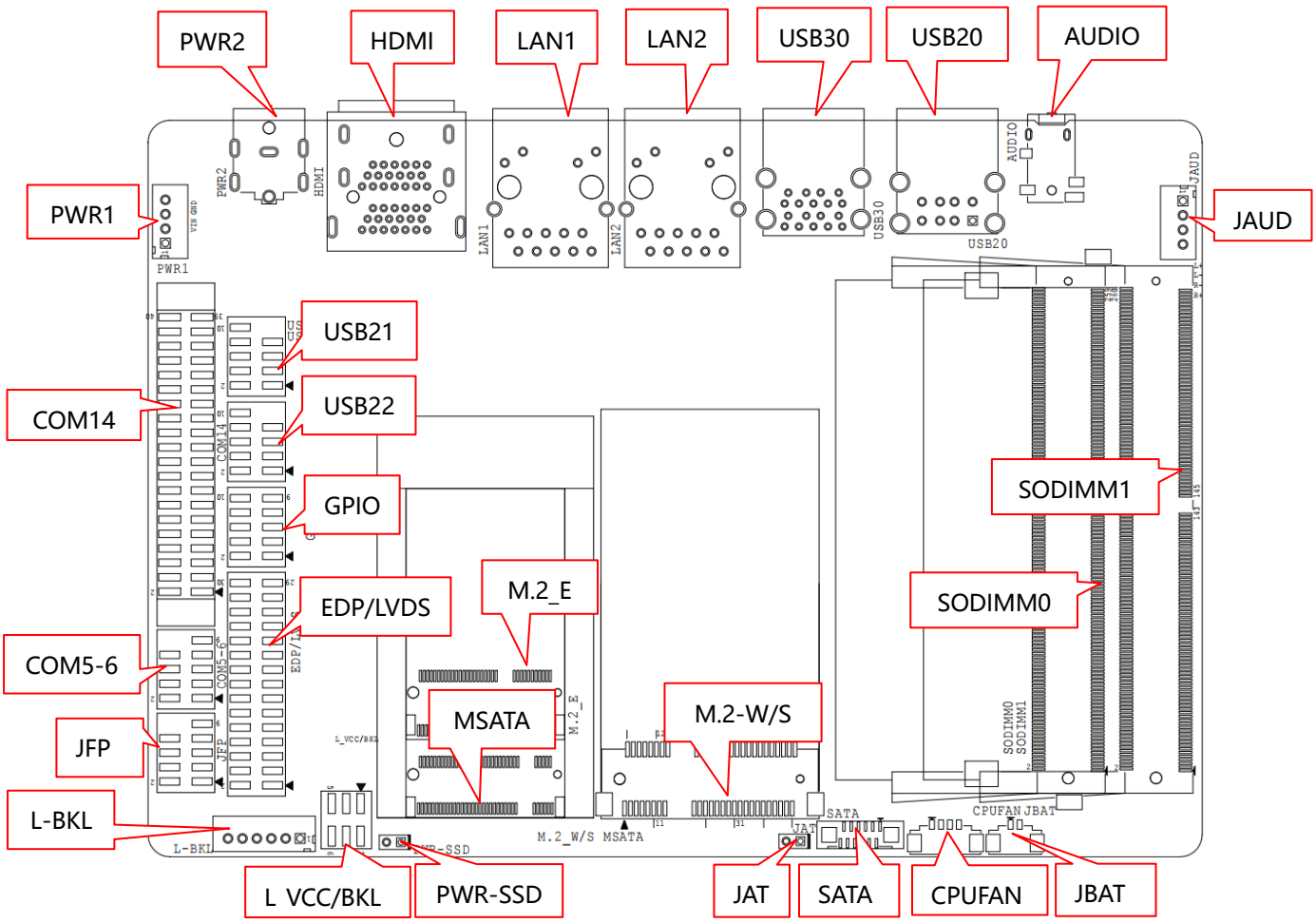
Power: 9V-35V DC-IN (5.5 × 2.5 mm)

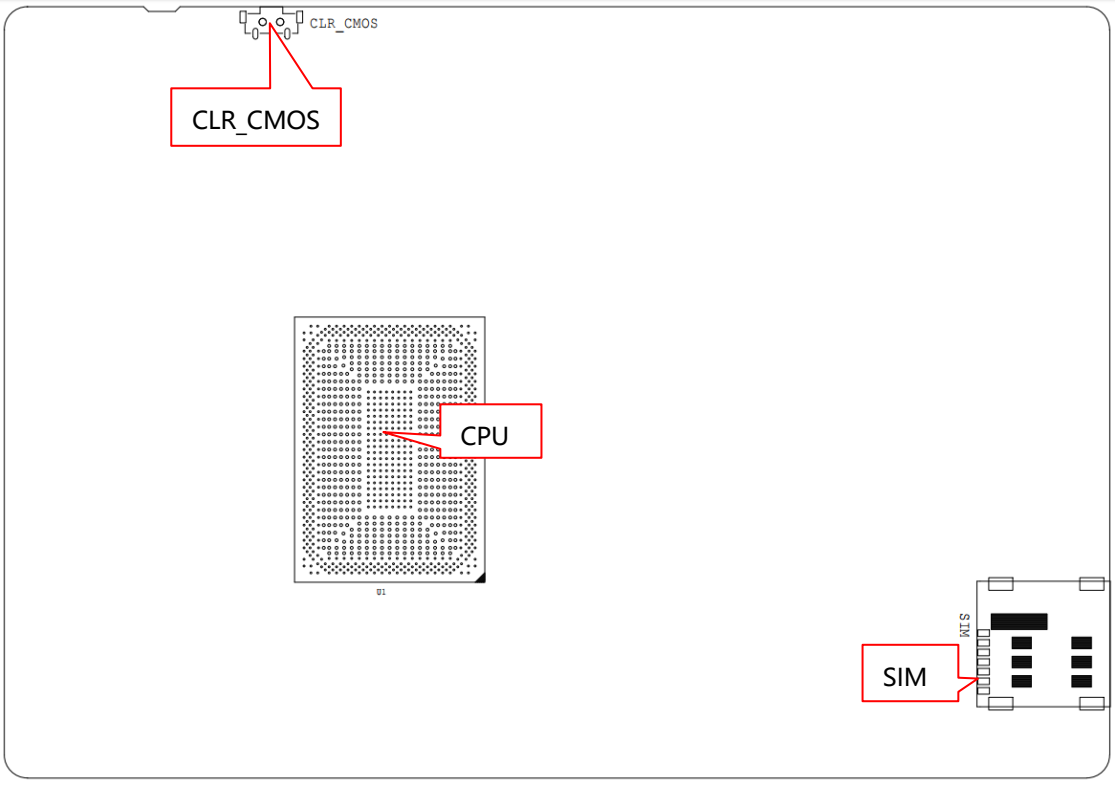
Operating Temperature: -20℃~60℃

Form Factor: 3.5” SBC

Dimension: 146mm x 102mm

1.3 Connector Diagram





Chapter 2 Hardware

2.1 Installations

Please refer to the following steps for installation:

1. Read the user manual carefully to make sure all the adjustments on the FP535 are correct.
2. Installing the Memory:
   - Press the ejector tab of the memory slot outwards with your fingertips.
   - Hold the memory module and align the key to the module with that on the memory slot.
   - Gently push the module into the slot until the ejector levers return completely to the closed position, holding the module in place when the module touches the bottom of the slot. To remove the module, press the ejector levers outwards to unseat the module.
3. Installing the expansion cards:
   - Locate the expansion slots and remove the screw, insert the cards into the slot at a 45-degree angle then attach the screw to the expansion cards, gently press down on it then install the screw back.
4. Connect all signal wires, cables, panel control wiring, and power supplies.
5. Start the computer and complete the setup of the BIOS program.

The board's components are integrated circuits and can easily be damaged by Electrostatic Discharge or ESD; therefore, please follow the instructions:

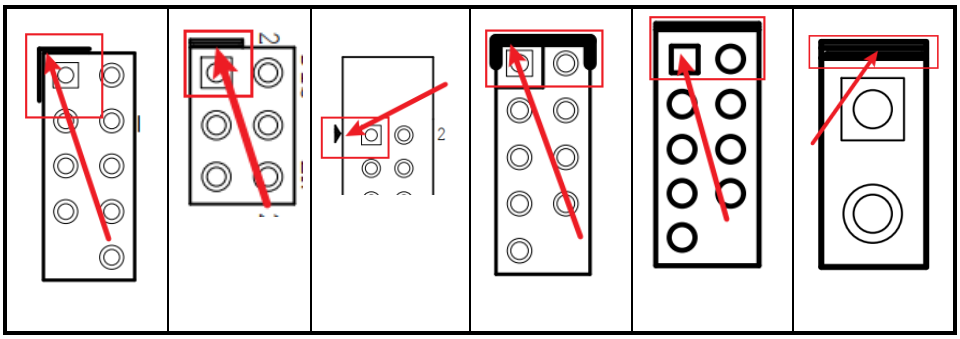
- Hold the board's edge when handing, and do not touch onboard pins, components, or plug sockets.
- When touching integrated circuit components (such as CPU, RAM, etc.), please wear an anti-static wrist strap/glove to avoid electrostatic discharge damage to the board or other sensitive components.
- Before installing the integrated circuits/sensitive components, place the sensitive components in anti-static bags to keep them safe from ESD.
- Please make sure the power switch is OFF before plugging the power plug.

2.2 Jumper Setting

Please configure the jumpers according to your requirements before installing the hardware.

How to identify the first header of jumpers and pins: Observe the mark beside the jumper or pins and find the header marked by “1” or bold line or triangular symbol. Or observe the rear panel and the header with a square solder pad is the first header.

Illustration:



2.3 Memory

The board provides 2x DDR4-2400/2667 MHz SO-DIMM slots, supporting dual-channel with a maximum total capacity of 64 GB.

Ensure the memory module is aligned with the slot key before insertion. When selecting memory, verify that the module meets the required specifications.

Please Note: When using dual-rank (dual-sided) memory modules with a total of 16 memory dies, the AMD Embedded R2314 processor supports a maximum memory frequency of 2400 MHz. When using dual-rank modules with a total of 8 memory dies, or single-rank (single-sided) modules with a total of 4 memory dies, the maximum supported memory frequency is 2667 MHz. For additional details, refer to the relevant sections of the AMD processor development documentation.

R2000 MAX DDR4 DATA RATE

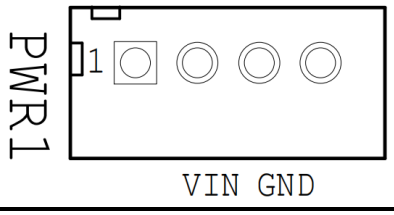
AMD

SO-DIMM OR UDIMM

SoC TDP	Memory Rank	Number of DIMM Socket on Each Channel	Max Data Rate (MT/s)
R2544	Single Rank	1	DDR4-3200
	Dual Rank	1	DDR4-2400
R2314 & R2514	Single Rank	1	DDR4-2667
	Dual Rank	1	DDR4-2400
R2312	Single Rank	1	DDR4-2400
	Dual Rank	1	DDR4-2400

2.4 Board Power Supply (Labeled PWR1, PWR2 onboard)

Supports power supply via a 5.5x2.5mm DC adapter (optional) rated for 9-35V; or via PH4 (4-pin) (2.0mm) power supply.

PWR2: 5.5 × 2.5 mm DC power input	PWR1: PH4 (4-pin, 2.0 mm) power connector
	

Power Measurement Notice

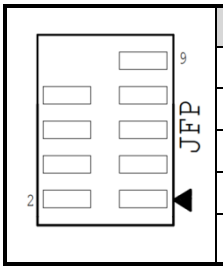
*The **AMD Ryzen™ Embedded R2314 processor** is not fully supported by most third-party hardware detection or monitoring software currently available. As this processor is designed for industrial and embedded applications, many **consumer-grade monitoring tools have not been fully calibrated** for it and may report inaccurate power consumption values. For accurate power readings, refer to the PM tab of the **AMD_SystemDeck_Tool (Windows)** provided by AMD.*

In internal testing with the BIOS power setting configured to 15 W, monitoring software may report approximately 6 W under stable load; however, the actual CPU power consumption is approximately 12–15 W.

2.5 Power Switch Connector (labeled as JFP on board)

The front panel connector provides interfaces for power switch, reset switch, and status indicators located on the chassis front panel.

Front Panel Pin Definition (labeled as JFP on board)



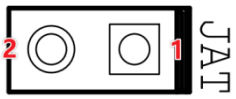
Signal	Pin		Signal
(null)	10	9	NC
PWR_ON-	8	7	RSTBTN+
PWR_ON+	6	5	RSTBTN-
PWR_LED-	4	3	HDD_LED-
PWR_LED+	2	1	HDD_LED+

2.6 Hardware Auto Power-On (labeled JAT onboard)

The **JAT** header (labeled **JAT** onboard) controls the hardware power-on auto-start function. Install the appropriate jumper to enable or disable this feature.

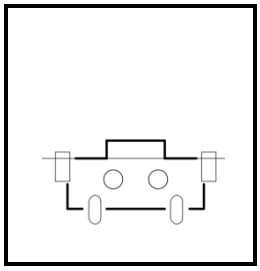
JAT Settings:

Enable	Disable
1-2	NC



2.7 CMOS Clearance/Retention (labeled CLR_CMOS onboard)

CLR_CMOS Button: Clears the CMOS settings. Labeled CLR_CMOS on board.



The CMOS is powered by onboard button batteries. Clearing CMOS will permanently remove the previous system settings and restore the board system to original settings (factory settings).

Steps:

1. Shut down the system and disconnect the power supply.
2. Press and hold the CLR_CMOS button for more than 3 seconds.
3. Power on the system and press <Del> during startup to enter the BIOS. Press F9 to load the optimal default settings, then save and exit.

⚠ Caution: Do not clear the CMOS while the system is powered on, as this may damage the motherboard.

2.8 Display Interfaces

The board provides multiple display outputs, including 2x HDMI2.0b, and 1x LVDS (optionally configurable as eDP):

- 2 × HDMI 2.0b port supporting up to 4K @ 60 Hz
- 1 × LVDS header (optional upgrade to eDP) supporting up to 1920 × 1200, 24-bit.
  When configured as an eDP interface (optional), the header supports 3.3V eDP panels up to 4K @ 30 Hz.

Please Note: *The LVDS/eDP signal is disabled by default. When enabled, the LVDS/eDP display becomes the primary display output, and the BIOS interface is displayed only on the LVDS/eDP screen. During this time, other display outputs (such as HDMI) will not show the BIOS screen. Before connecting an LVDS display, ensure that the panel parameters are configured correctly. If incorrect parameters are applied, the system must be reset by clearing the CMOS before reconfiguring the display settings.*

2.8.1 LVDS (Labeled EDP/LVDS, L-BKL, L-ADJ/DIS, L_VCC onboard)

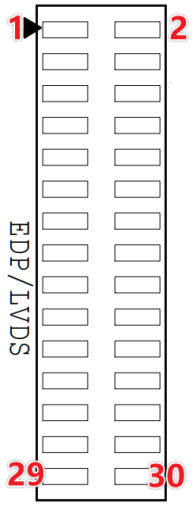
When the interface is configured for LVDS mode, the following headers operate as LVDS-related control and power interfaces:

EDP/LVDS: Carries the LVDS signal lines.

L-BKL: Controls panel backlight on/off and brightness adjustment.

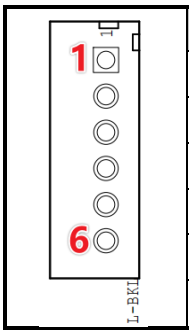
L-VCC / L-BKL: Provides LCD operating voltage selection and backlight polarity (forward/inversion) control.

LVDS Data Pin (labeled EDP/LVDS onboard) (2.0mm):



Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	GND
GND	5	6	GND
A_DATA0_DN	7	8	A_DATA0_DP
A_DATA1_DN	9	10	A_DATA1_DP
A_DATA2_DN	11	12	A_DATA2_DP
GND	13	14	GND
A_CLK_DN	15	16	A_CLK_DP
A_DATA3_DN	17	18	A_DATA3_DP
B_DATA0_DN	19	20	B_DATA0_DP
B_DATA1_DN	21	22	B_DATA1_DP
B_DATA2_DN	23	24	B_DATA2_DP
GND	25	26	GND
B_CLK_DN	27	28	B_CLK_DP
B_DATA3_DN	29	30	B_DATA3_DP

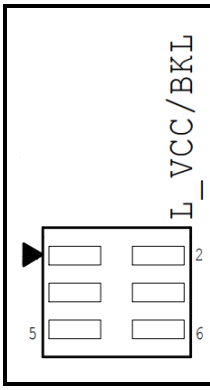
LVDS Backlight Connector Pin (Labeled L-BKL onboard):



Pin	Signal
1	GND
2	GND
3	LCD_BKL_ADJ
4	LCD_BKL_ON
5	12V
6	12V

LVDS Operating Voltage and Backlight Polarity Adjustment Pin (Labeled L_VCC/BKL onboard):

The **L_VCC/BKL** pin is used to configure the LVDS operating voltage and backlight polarity.



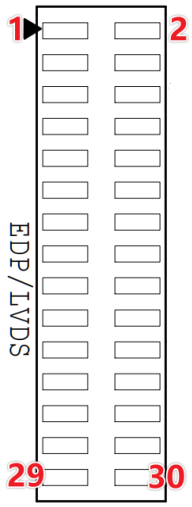
Pin	Setting	Function
1-3	Close	VCC(+3.3V)
3-5	Close	VCC(+5V)
2-4	Close	REV (Backlight Control Reverse)
4-6	Close	STD (Backlight Control Standard)

Please Note: *The LVDS operating voltage adjustment switch is pin controlled. By shorting the jumper caps, the voltage can be flexibly adjusted between 3.3V/5V. Based on your LVDS display's voltage parameters, use the jumper caps to short the pins corresponding to the required voltage. (Do not short pins of different voltages simultaneously.)*

2.8.2 eDP (optional)

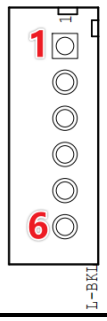
When set to eDP mode, the “EDP/LVDS” pins output eDP signals. The “L-BKL” pins are used for backlight control, and the “L-ADJ/DIS” pins provide power to the panel and backlight (with forward/inversion adjustment).

eDP Data Pins (labeled EDP/LVDS onboard) (2.0mm):



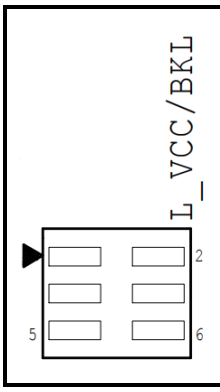
Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	EDP_HPD
GND	5	6	GND
EDP_AUXN	7	8	EDP_AUXP
N/A	9	10	N/A
EDP_DATA0_P	11	12	EDP_DATA0_N
GND	13	14	GND
N/A	15	16	N/A
EDP_DATA1_P	17	18	EDP_DATA1_N
N/A	19	20	N/A
N/A	21	22	N/A
N/A	23	24	N/A
GND	25	26	GND
N/A	27	28	N/A
N/A	29	30	N/A

eDP Backlight Connector Pin (labeled L-BKL onboard):



Pin	Signal
1	GND
2	GND
3	LCD_BKL_ADJ
4	LCD_BKL_ON
5	12V
6	12V

eDP Operating Voltage and Backlight Polarity Adjustment Pin(Labeled L_VCC/BKL onboard):

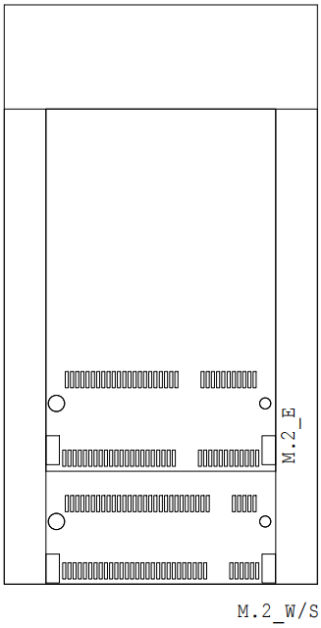
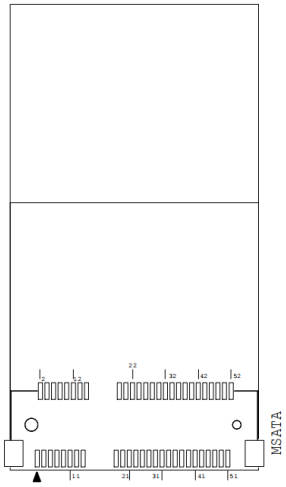
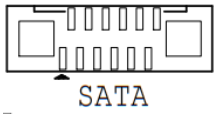


Pin	Setting	Function
1-3	Close	VCC(+3.3V)
3-5	Close	VCC(+5V)
2-4	Close	REV (Backlight Control Reverse)
4-6	Close	STD (Backlight Control Standard)

Please Note: *The eDP operating voltage adjustment switch is pin controlled. Jumper caps can be used to flexibly adjust between 3.3V/5V. Based on your eDP display's voltage specifications, use jumper caps to short the pins corresponding to the required voltage. (Do not short pins of different voltages simultaneously.)*

2.9 Storage Interfaces (Labeled M.2_W/S/MSATA/SATA onboard)

- 1xmSATA slot (labeled MSATA onboard)
- 1xM.2 Key B slot supporting 2242 SATA SSDs, 3042 4G modules, or 3052 5G modules (labeled M.2_W/S onboard)
- 1xFPC SATA slot (optional) (either the M.2_W/S slot or the FPC SATA slot can be used, as they share one signal channel) (labeled SATA onboard)

M.2_W/S	MSATA	SATA
		

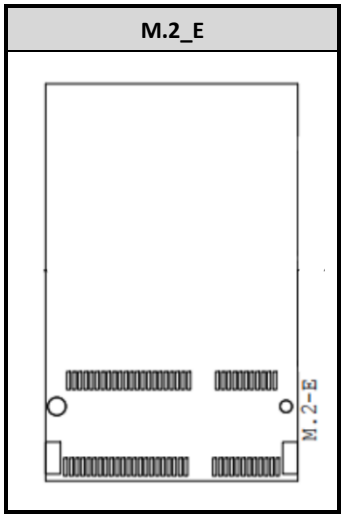
PWR-SSD: (Insert the corresponding jumper cap to select the appropriate module type.)

Function Selection	Jumper Setting
SSD / 4G module	Pins 1-2 shorted
5G module	NC
	

Please Note: *When installing an **M.2 Key B 2242 SATA SSD** in the **M.2_W/S** slot, the **PWR-SSD** jumper cap must be installed to select the correct voltage. Failure to do so may damage the SSD or 4G module.*

2.10 Expansion Slots (Labeled M.2_E onboard)

- 1 × M.2 Key E slot, supporting 2230 Wi-Fi & Bluetooth modules (PCIe / USB 2.0); labeled M.2_E onboard.



2.11 USB Interface (Labeled USB30, USB20, USB21, USB22)

The board provides the following USB ports:

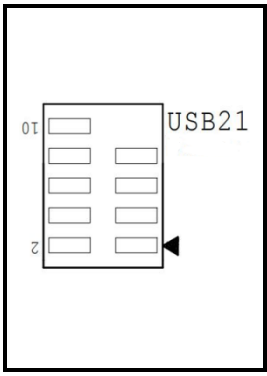
- 2 × USB 3.2 Gen 2 Type-A ports (10 Gbps) — labeled USB30 onboard
- 5 × USB 2.0 ports (480 Mbps), including:
  - 2 × USB 2.0 Type-A rear ports (labeled as USB20 on board).
  - 3 × USB 2.0 via onboard pin headers (labeled as USB21/USB22 on board, 2.0 mm pitch), with 2 ports routed from USB21 and 1 port routed from USB22.

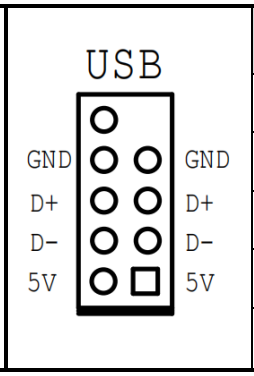
The rear 4xUSB Type-A ports (labeled USB30/USB20 on board) are powered by the 5V system supply. Controlled by the CPU S5 power signal, these ports support system wake-up from sleep or hibernation via a connected USB keyboard or mouse, while also supplying power to external devices. The 2xUSB 3.2 Gen 2 Type-A ports provide 5V/1A, and two USB 2.0 Type-A ports provide 5V/0.5A.

Please Note:

1. Windows 10 and later operating systems: when Fast Startup is enabled, the USB interfaces remain powered after shutdown. When Fast Startup is disabled, the USB interfaces are powered off after shutdown.
2. Linux operating systems: USB power is disabled when the system is shut down.
3. The USB 3.2 Gen 2 Type-A ports (labeled “USB30” on board) can be optionally configured to provide 5V standby power. In any system state (e.g., soft shutdown without power loss or sleep mode), connecting a USB keyboard or mouse to the corresponding port can wake the system and supply power to external devices at 5V/1A.

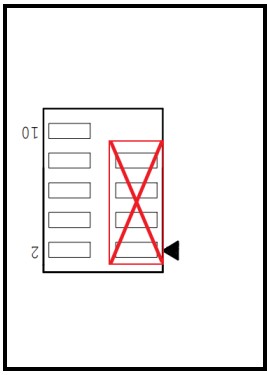
USB Pin Definition: (labeled USB21 on board)

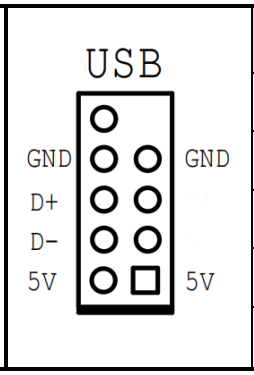




Signal	Pin		Signal
NC	10	9	(Null)
GND	8	7	GND
USB DATA+	6	5	USB DATA+
USB DATA-	4	3	USB DATA-
VCC 5V	2	1	VCC 5V

USB Pin Definition: (labeled USB22 on board)

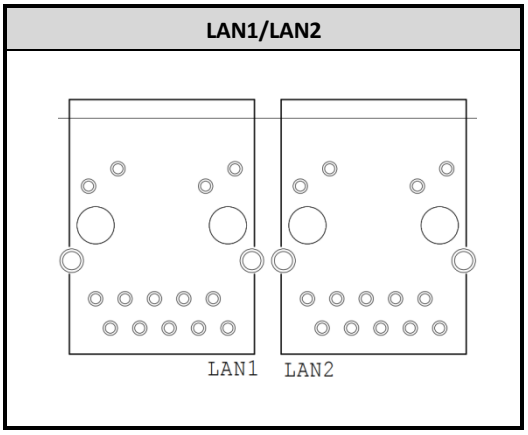




Signal	Pin		Signal
NC	10	9	(Null)
GND	8	7	GND
USB DATA+	6	5	(Null)
USB DATA-	4	3	(Null)
VCC 5V	2	1	VCC 5V

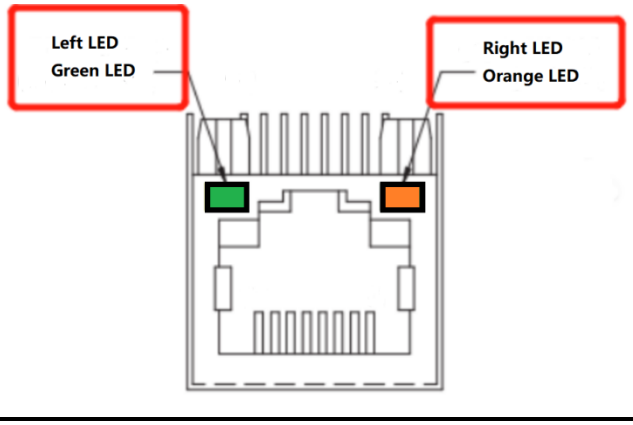
2.12 LAN (labeled LAN1/LAN2 onboard)

The motherboard is equipped with the Realtek® RTL8111H Gigabit Ethernet controller, providing two RJ45 LAN interfaces (labeled LAN1 / LAN2 onboard). Both ports support Wake-on-LAN (Magic Packet wake-up), while LAN1 additionally supports PXE network boot. When using UEFI PXE boot, set IPv4 PXE Support = “Enabled” in the BIOS, “disabled” by default.



LED Status Indicators:

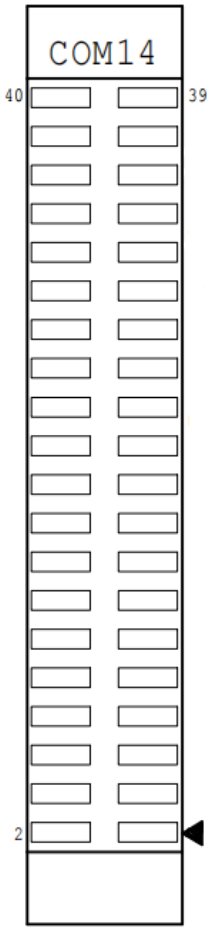
LI_LED (Green)	Function	ACT_LED (Orange)	Function
Always on	Network connected	Blinking	Data transfer active



2.13 Serial Ports (Labeled COM14， COM5-6 onboard)

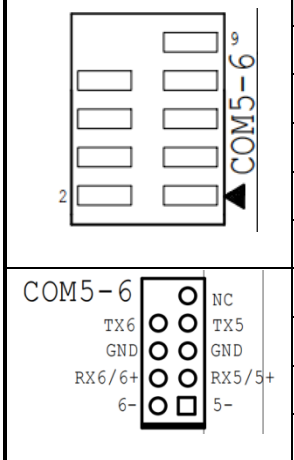
The board features two sets of serial port headers (2.0mm), providing 4xRS232(labeled COM1_4 onboard, with 12V powered) serial ports and 2xRS485(labeled COM5_6 onboard) serial ports by default, and the COM5_6 can be configured for RS-232 operation through designated hardware modification.

COM14(labeled COM14 onboard)



Signal	Pin		Signal
12V	40	39	RI#
CTS#	38	37	RTS#
DSR#	36	35	GND
DTR#	34	33	TXD
RXD	32	31	DCD#
12V	30	29	RI#
CTS#	28	27	RTS#
DSR#	26	25	GND
DTR#	24	23	TXD
RXD	22	21	DCD#
12V	20	19	RI#
CTS#	18	17	RTS#
DSR#	16	15	GND
DTR#	14	13	TXD
RXD	12	11	DCD#
12V	10	9	RI#
CTS#	8	7	RTS#
DSR#	6	5	GND
DTR#	4	3	TXD
RXD	2	1	DCD#

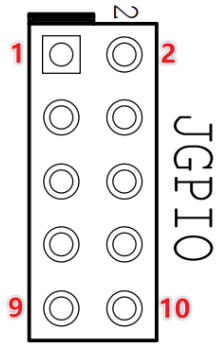
COM5-6 Pin Definition: (Labeled COM5-6 onboard)



Pin	RS232(Optional)	RS485
1	NC	COM5_DATA-
2	NC	COM6_DATA-
3	RX5	COM5_DATA+
4	RX6	COM6_DATA+
5	GND	GND
6	GND	GND
7	TX5	(NC)
8	TX6	(NC)
9	NC	(NC)

2.14 GPIO (Labeled GPIO onboard)

The motherboard provides a 2×5-pin JGPIO header (**Labeled GPIO onboard, 2.0 mm pitch**), providing eight programmable GPIO ports. Please refer to the appendix for GPIO configuration details.



Signal	Pin		Signal
SIO_GP70	1	2	3.3V
SIO_GP71	3	4	SIO_GP74
SIO_GP72	5	6	SIO_GP75
SIO_GP73	7	8	SIO_GP76
GND	9	10	SIO_GP77

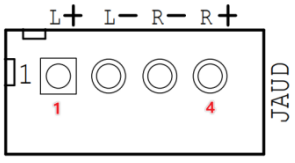
2.15 Audio (labeled AUDIO, JAUD onboard)

The motherboard integrates the SenaryTech SN6186 High-Definition Audio codec and supports one 3.5 mm CTIA combo audio jack (Line-out + Mic-in), **labeled AUDIO on board**.

In addition, the board provides a built-in dual-channel amplifier output for connecting passive speakers. The amplifier output is available through the JAUD **(labeled JAUD on board)** header (2.0 mm pitch).

CTIA combo audio jack (Line-out + Mic-in in one):

JAUD Amplifier Output Header (Labeled JAUD onboard, 2.0mm):

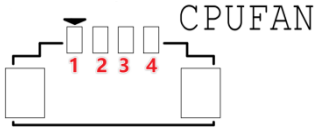


Pin	Signal
1	L+
2	L-
3	R-
4	R+

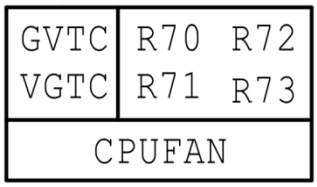
2.16 CPU Fan/System Fan Socket (Labeled CPUFAN onboard)

The motherboard provides **one 5 V, 4-pin fan header** (1.25 mm pitch), labeled **CPUFAN** on the motherboard. This connector supports both CPU fan and system fan operation.

CPU Fan Definition (Labeled CPUFAN onboard):



Default Configuration (Resistors R71 and R73 populated)				
Pin	1	2	3	4
Signal	5V	GND	TAC	CTL



Optional Configuration (Resistors R70 and R72 populated)				
Pin	1	2	3	4
Signal	GND	5V	TAC	CTL

Chapter 3 BIOS Setup

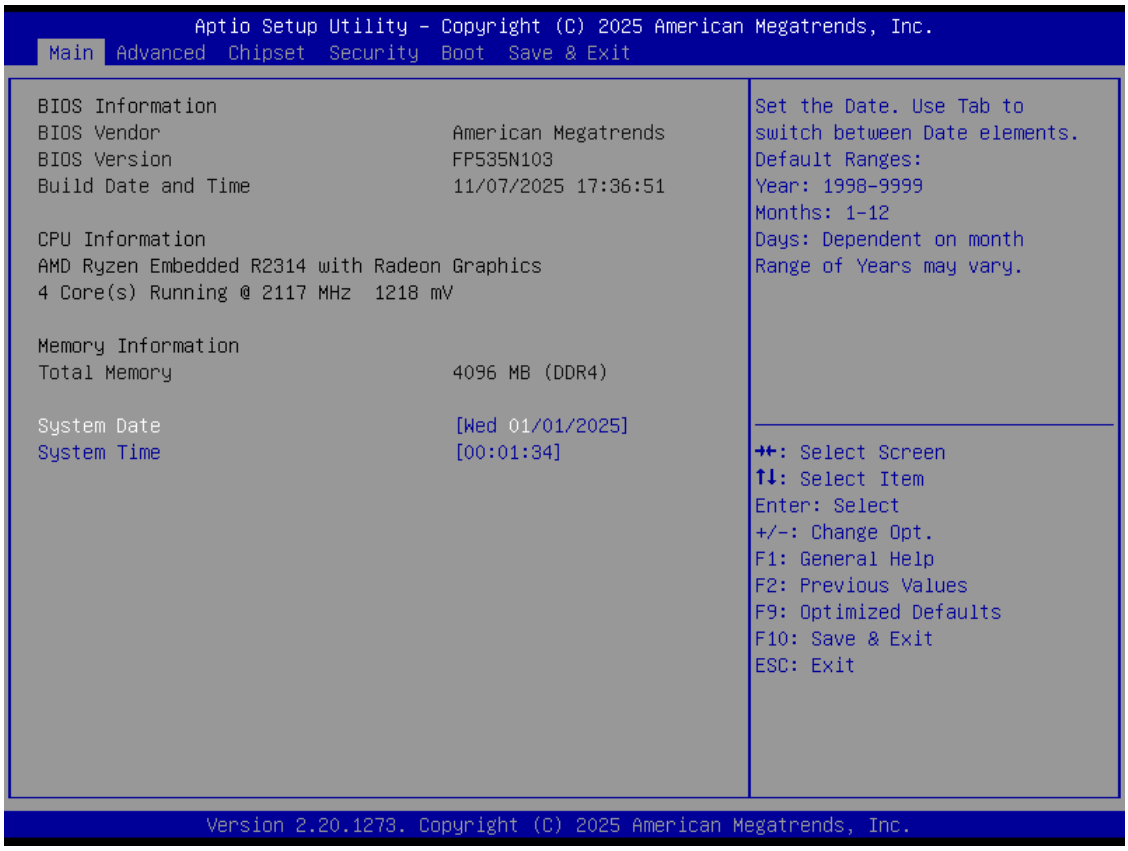
3.1 Entering the BIOS

1. Turn on the computer and press <Delete> entering the BIOS
2. BIOS Hotkey Functions

BIOS Hotkey Functions:

Key	Function	Description
→ ←	Select Screen	Navigate between menu screens.
↑↓	Select Item	Move between menu items or options.
Enter	Select	Open a submenu or confirm a selection.
+/-	Change Option	Adjust values or change settings.
F1	General Help	Displays helpful information for the selected item.
F2	Previous Values	Load the previously saved settings.
F9	Optimized Defaults	Restore factory default settings.
F10	Save & Exit	Save changes and exit BIOS.
ESC	Exit	Exit BIOS or return to the previous menu.

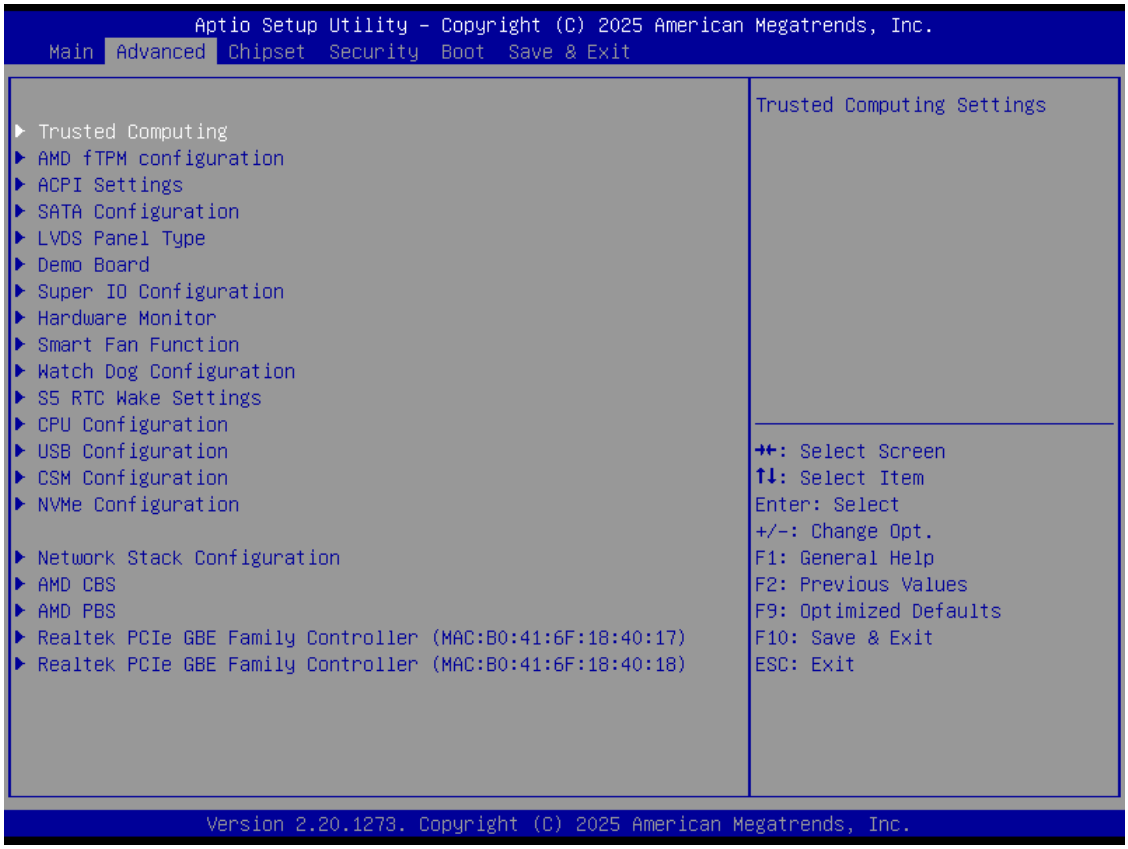
3.2 Main Menu （BIOS Info, Date, Time）



BIOS Information

- BIOS Vendor: American Megatrends
- BIOS Version: Displays the current BIOS version
- Build Date and Time: BIOS build timestamp
- Processor Information: CPU identification details
- Total Memory: Installed system memory
- Memory Frequency: Active memory operating frequency
- PCH Information: Platform Controller Hub details
- PCH SKU: PCH model identifier
- ME FW Version: Intel Management Engine firmware version
- System Date: System date setting (format: MM/DD/YYYY)
- System Time: System time setting (format: HH:MM:SS)

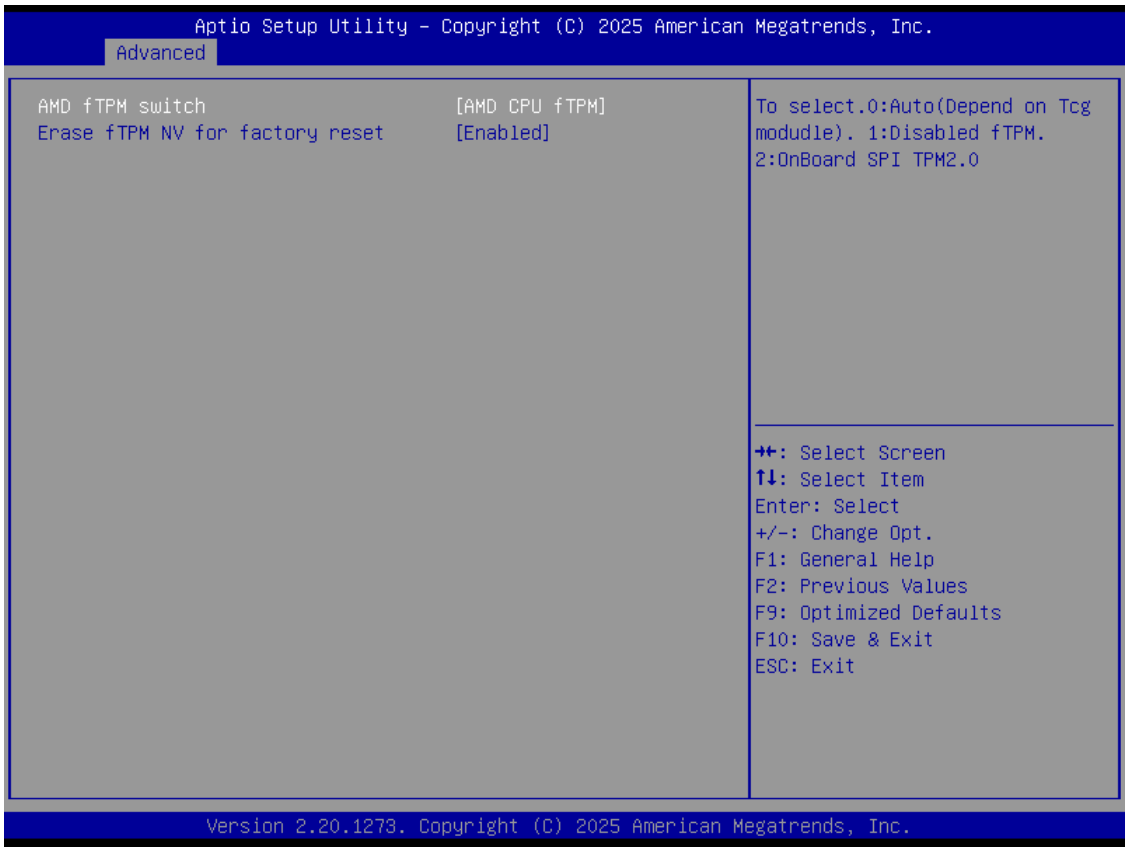
3.3 Advanced Settings



Selecting any item in the left pane opens its corresponding Advanced submenu. The Advanced section allows you to configure system features, adjust platform behavior, and modify CPU-related settings.

- **Trusted Computing:** AMD fTPM Configuration: Enables or disables AMD firmware TPM support.
- **ACPI Settings:** Configures ACPI power management states and system sleep behavior.
- **SATA Configuration:** Sets SATA controller operating mode and manages connected SATA devices.
- **LVDS Panel Type:** Selects the connected LVDS panel resolution and timing parameters.
- **Demo Board (Not supported):** Reserved for demo board functions; not supported on this platform.
- **Super I/O Configuration:** Configures legacy I/O interfaces such as serial ports and GPIO.
- **Hardware Monitor:** Displays system voltage, temperature, and fan speed information.
- **Smart Fan Function:** Controls fan speed behavior based on temperature thresholds.
- **Watchdog Configuration:** Configures the watchdog timer for system monitoring and automatic recovery.
- **S5 RTC Wake Settings:**Sets scheduled system power-on from the S5 (shutdown) state using the RTC.
- **CPU Configuration:**Configures processor features, cores, and power-related behavior.
- **USB Configuration:** Manages USB controller settings and legacy USB support.
- **CSM Configuration:** Configures Compatibility Support Module (legacy boot support).
- **NVMe Configuration (Not supported):** Reserved for NVMe device configuration; not supported on this platform.
- **Network Stack Configuration:** Enables network boot and configures PXE/UEFI network settings.
- **AMD CBS:** Provides advanced AMD CPU feature configuration (Common BIOS Settings).
- **AMD PBS:** Configures AMD platform-specific power and performance behavior.

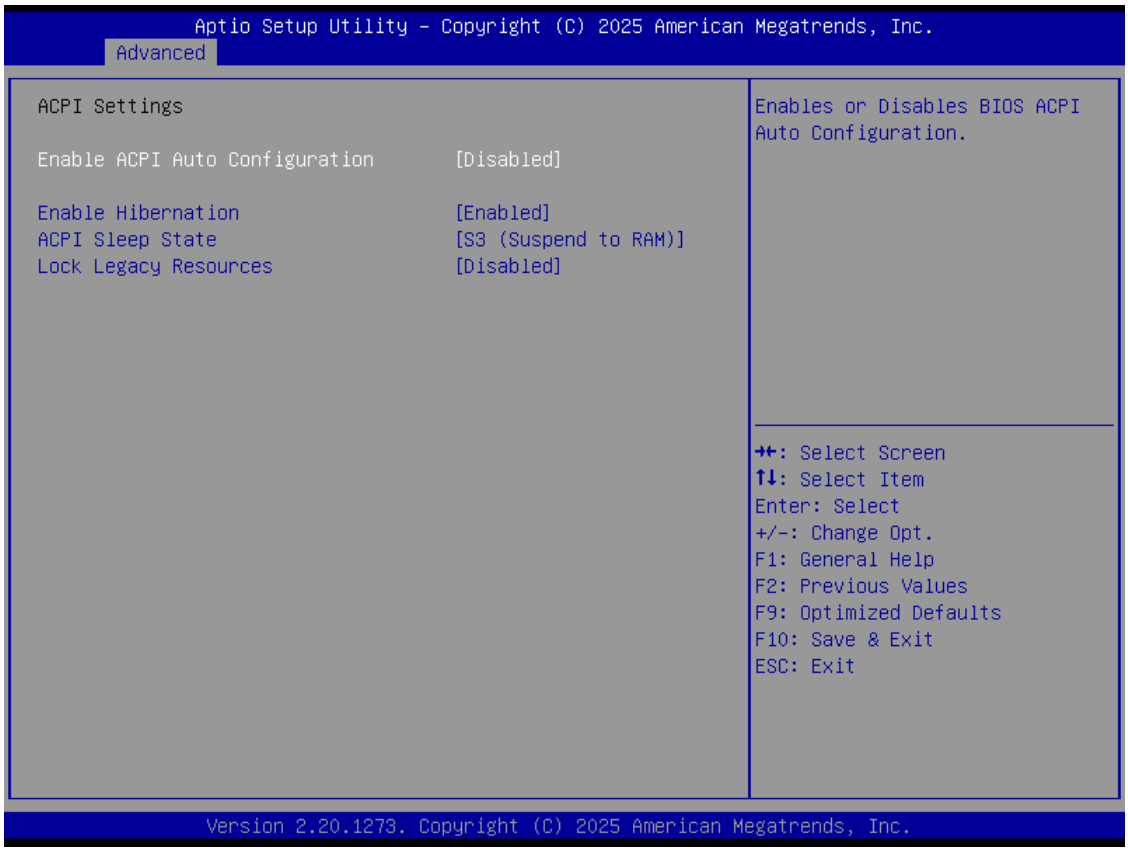
3.3.1 AMD fTPM configuration



AMD fTPM Configuration

- Erase fTPM NV for factory reset
    - Enable or disable fTPM reset for newly installed CPUs.
    - Default: Enabled

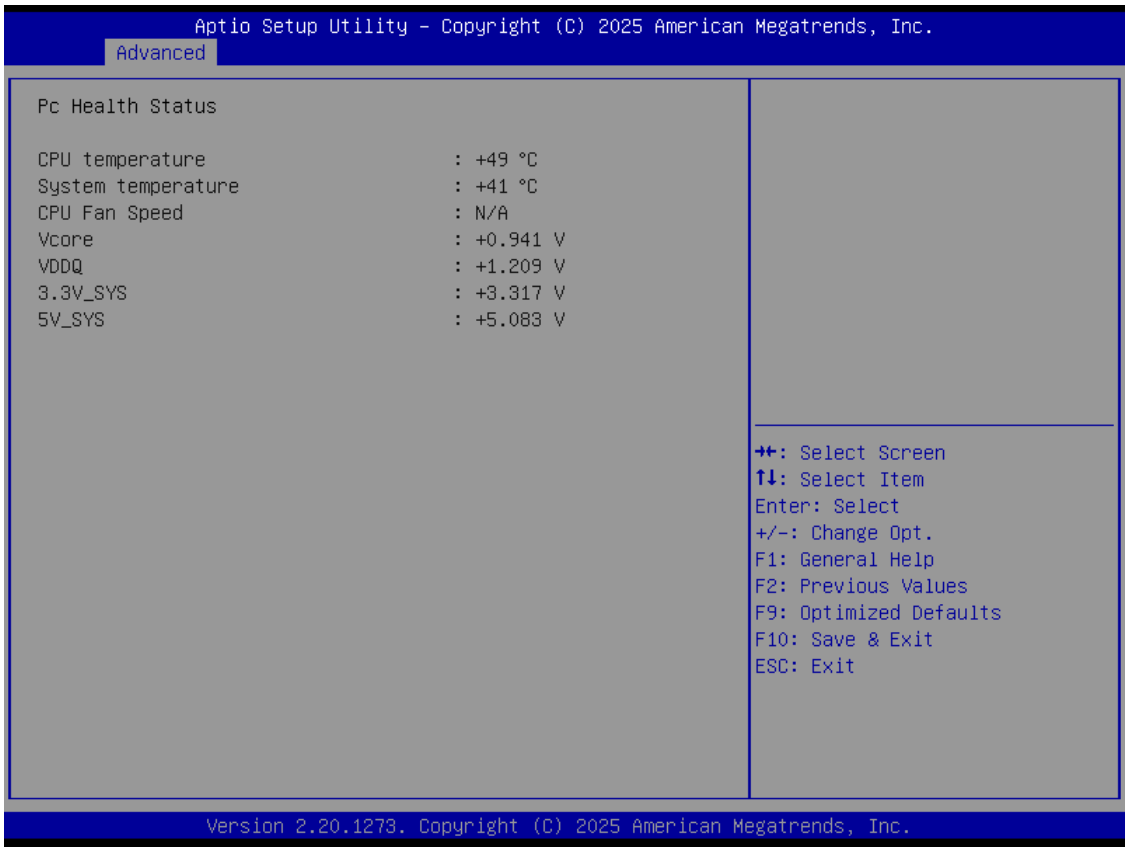
3.3.2 ACPI Settings



ACPI Settings

- **Enable ACPI Auto Configuration**: Enables or disables automatic ACPI configuration. Disabled by default.
- **Enable Hibernation**: Enables or disables system hibernation support.
- **ACPI Sleep State**: Selects the system ACPI sleep state.
- **Lock Legacy Resources**: Enables or disables locking of legacy system resource

3.3.3 Hardware Monitor

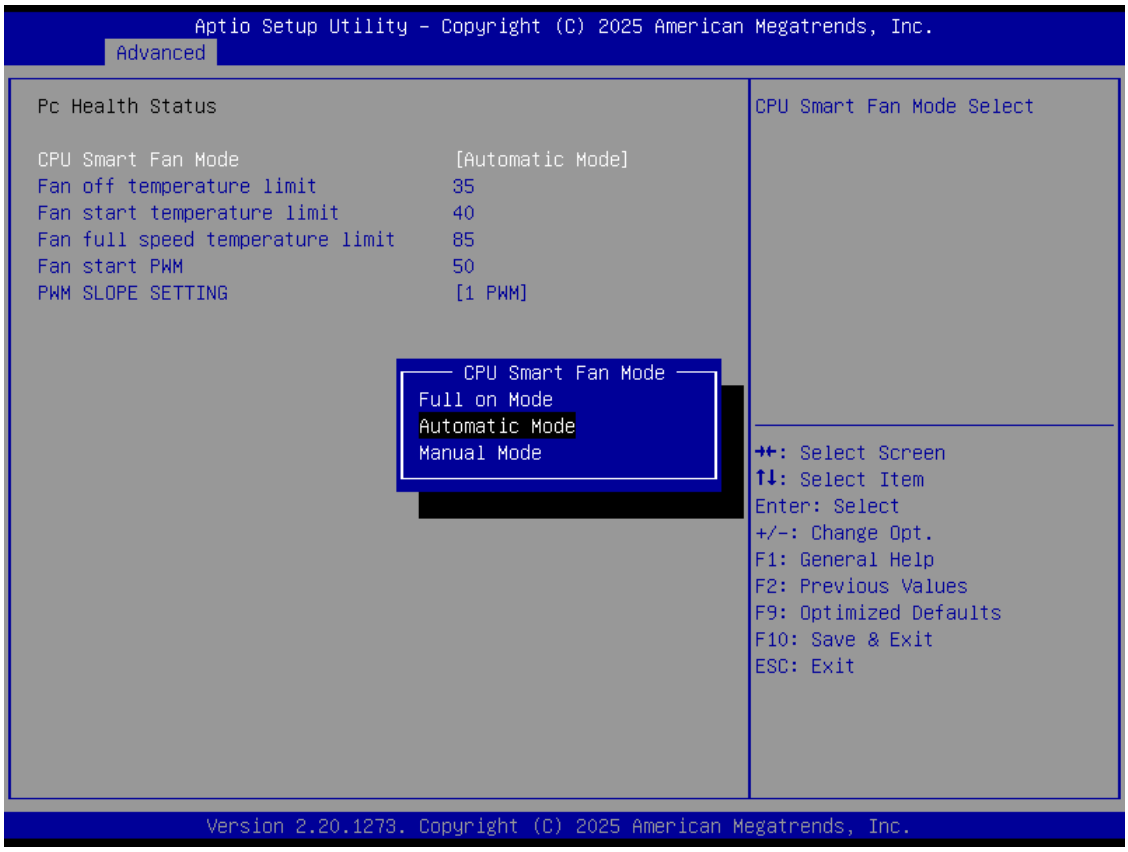


PC Health Status

The PC health status displays CPU temperature, system temperature, fan speed, and other relevant voltage values.

- **CPU Temperature:** Displays the current CPU temperature.
- **System Temperature:** Displays the current system temperature.
- **CPU Fan Speed:** Displays the current CPU fan speed.
- **System Fan Speed:** Displays the current system fan speed.
- **Vcore:** Displays the CPU core voltage.
- **V_DDQ:** Displays the memory I/O voltage.
- **3.3V_SYS:** Displays the system 3.3 V voltage.
- **5V_SYS:** Displays the system 5 V voltage

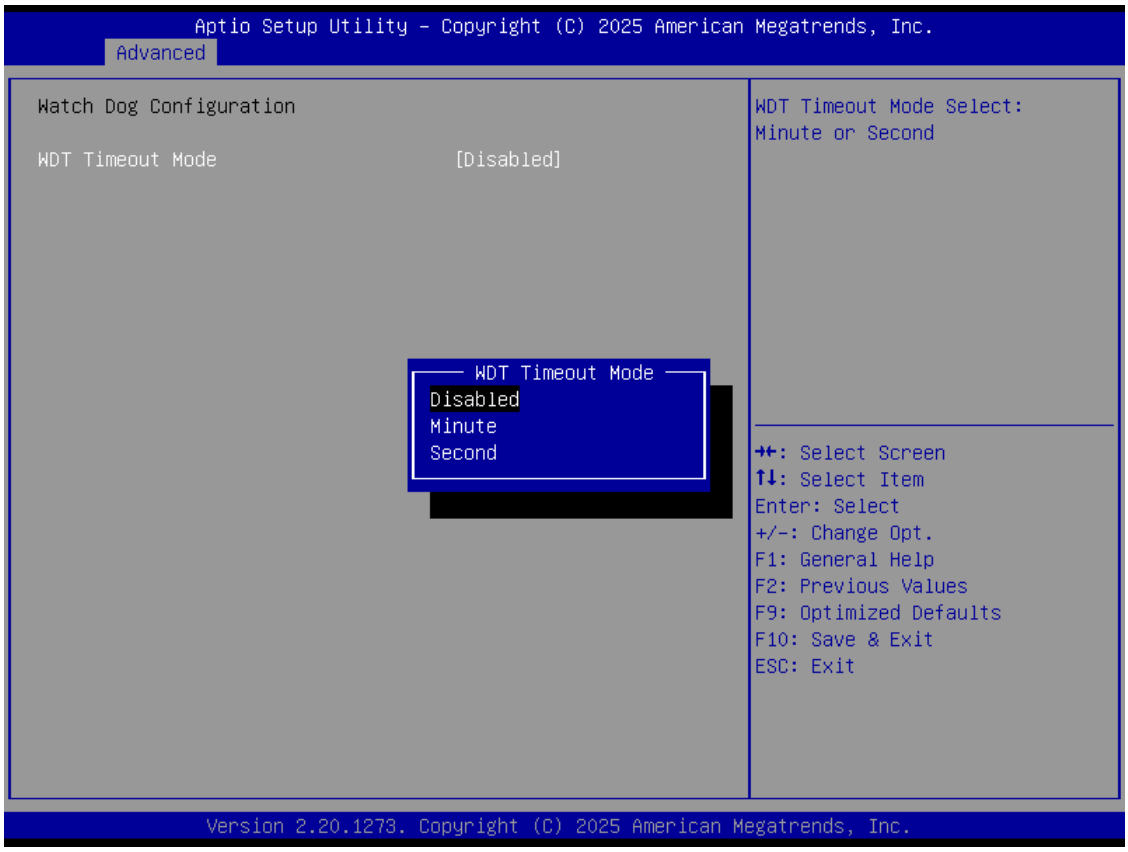
3.3.4 Smart Fan Function



PC Health Status → Smart CPU_Fan Mode

- **Smart CPU_Fan Mode / Smart SYS_Fan Mode:** Enables or disables smart fan control for the CPU fan or system fan.
- **Automatic Mode:** Automatically adjusts fan speed based on system temperature. (Default mode)
- **Full On Mode:** Forces the fan to operate at full speed continuously.
- **Manual Mode:** Allows manual configuration of fan speed control parameters.
- **Fan Off Temperature Limit:** the temperature threshold below which the fan stops.
- **Fan Start Temperature Limit:** the temperature at which the fan starts operating.
- **Fan Full Speed Temperature Limit:** the temperature at which the fan runs at full speed.
- **Fan Start PWM:** the initial PWM duty cycle when the fan starts.
- **PWM Slope Setting:** Adjusts the rate at which PWM duty cycle increases with temperature.

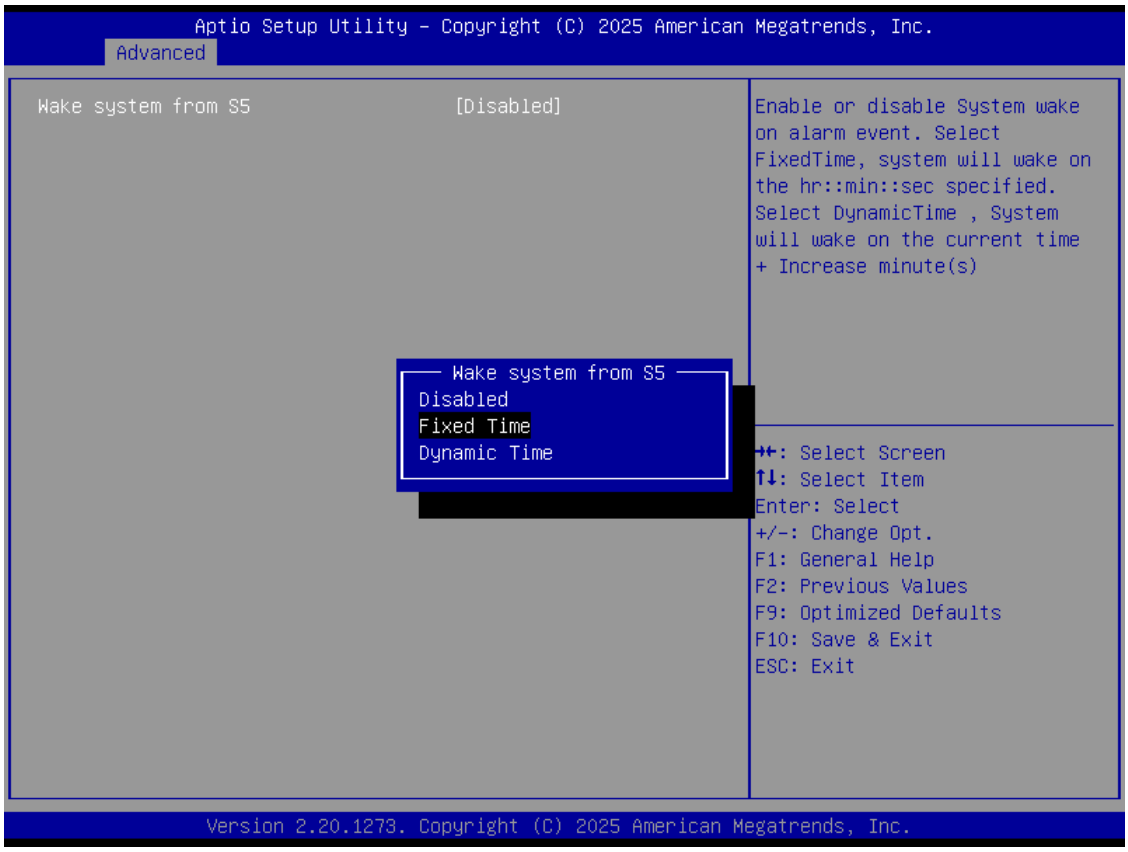
3.3.5 Watch Dog Configuration



Watch Dog Configuration

- WDT Timeout Mode: Select Minute or Second

3.3.6 S5 RTC Wake Settings



S5 RTC Wake Settings

- **Wake System From S5**: Enables or disables automatic system power-on from the S5 (shutdown) state.

  Default: Disabled

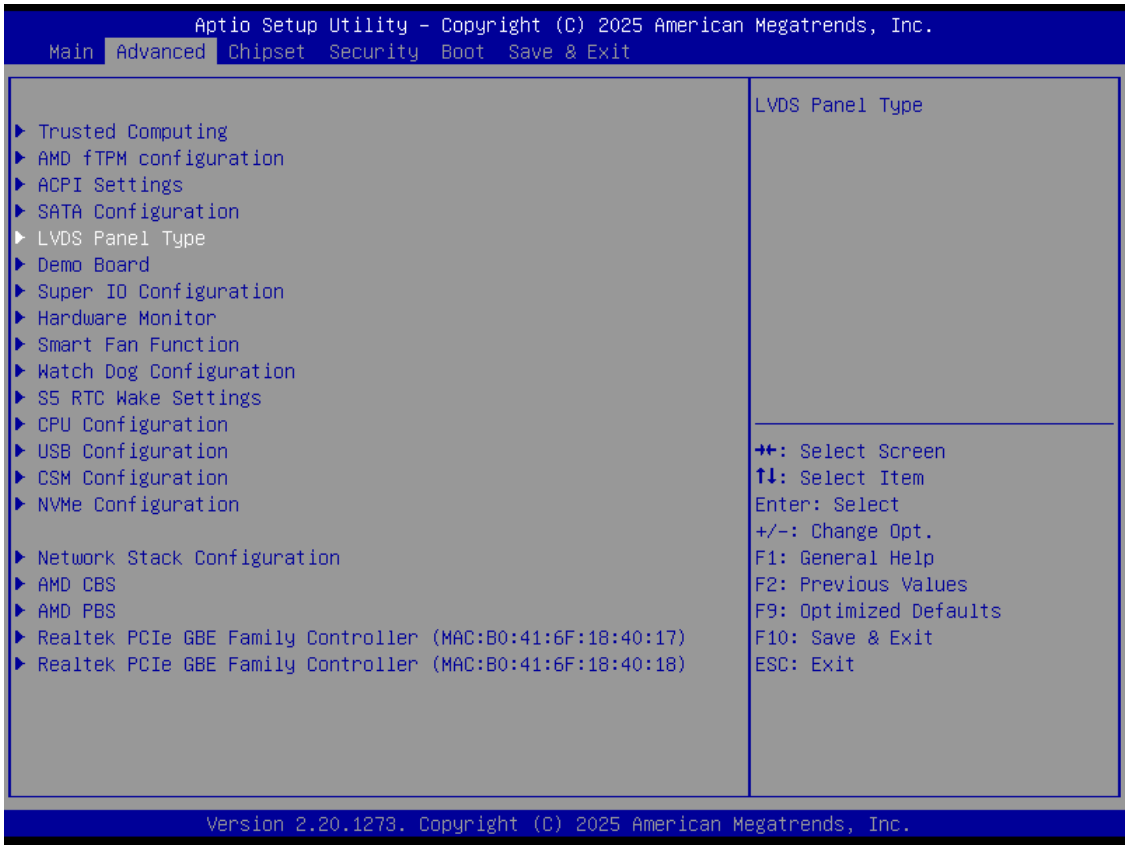
- **Wake Time Mode**: Selects the wake-up timing mode.
  - **Fixed Time**: When selected, the system wakes at the specified **Hour : Minute : Second**.
  - **Dynamic Time**: When selected, the system wakes after a dynamically calculated time interval.

3.3.7 LVDS Panel Type

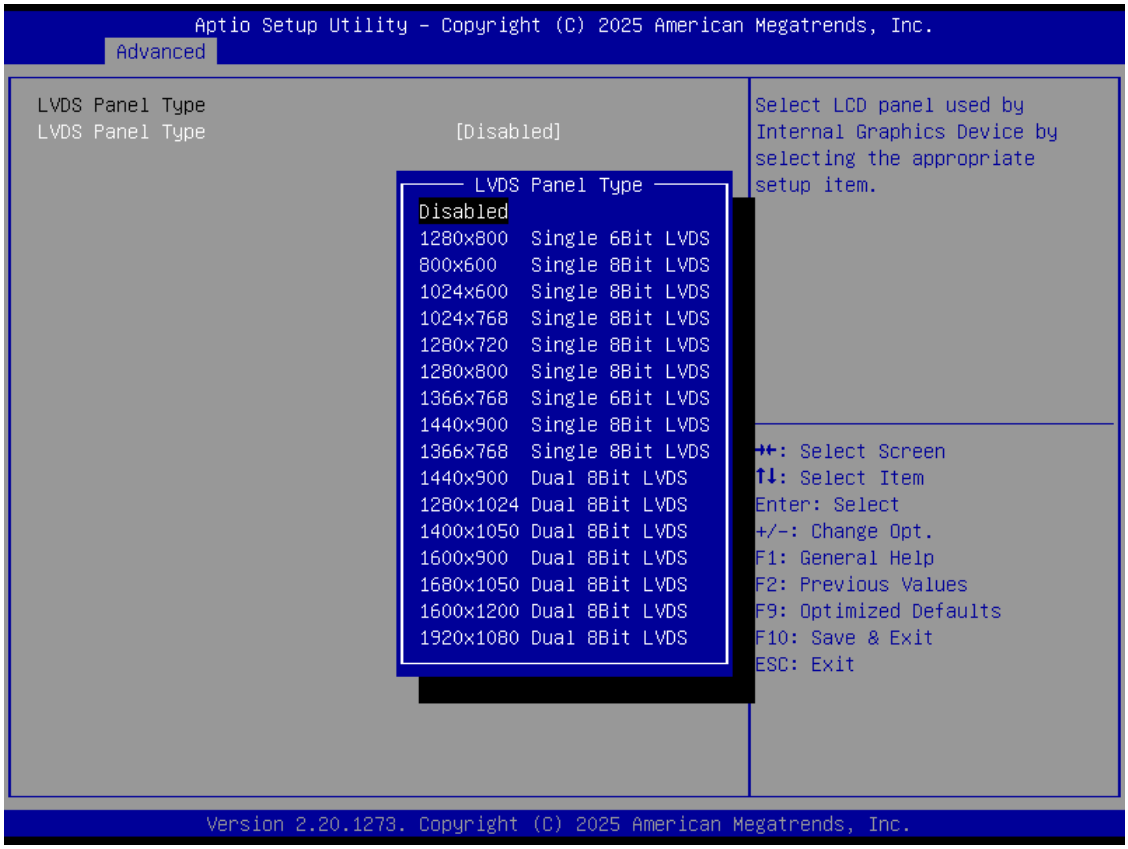
This menu is used to enable LVDS output and select the appropriate LCD panel parameters.

Configuration Steps:

- Power on the system and press Delete to enter the BIOS Setup Utility.
- Navigate to Advanced → LVDS Panel Type, then press Enter.



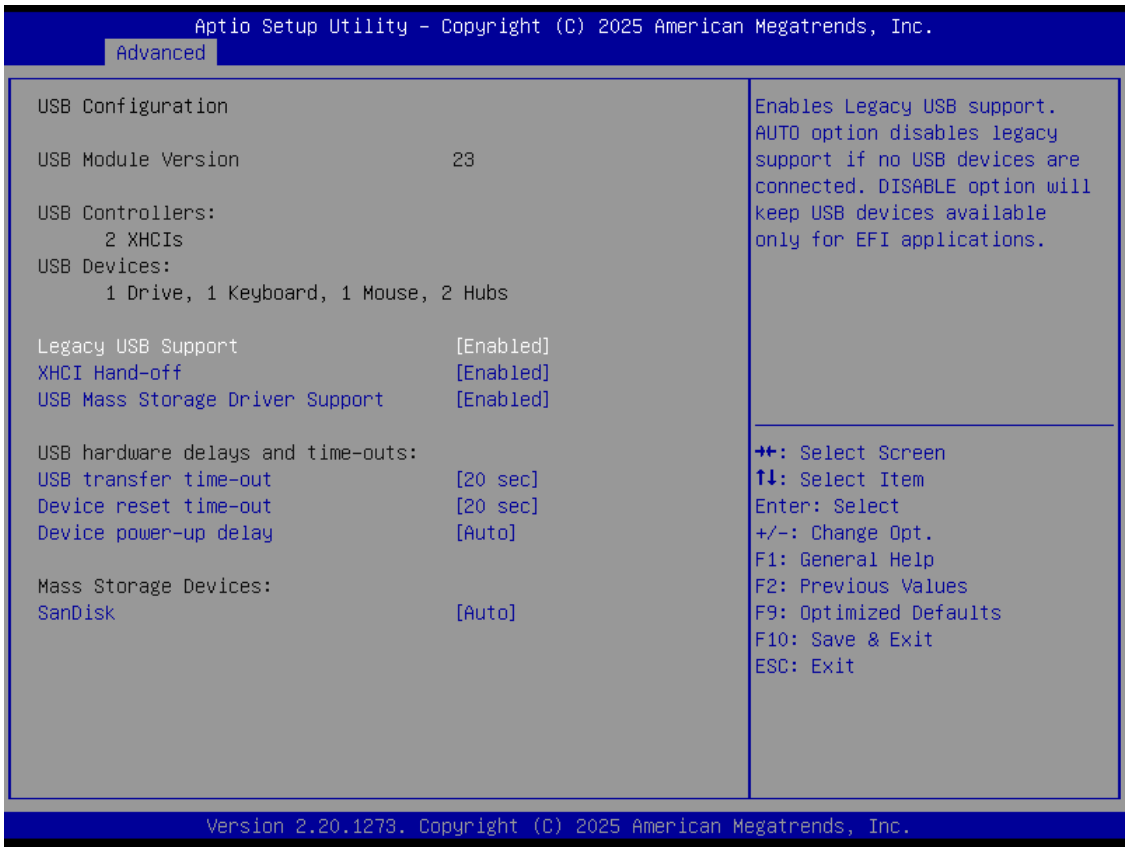
- Select **LCD Panel Type**.
    1. The default setting is **Disabled**, which turns off LVDS output.
    2. Select the required LVDS resolution to enable LVDS. Panel parameter options correspond to the LCD panel specifications (such as resolution, color depth, and channel configuration). Configure the setting according to the panel's specification sheet.



Note

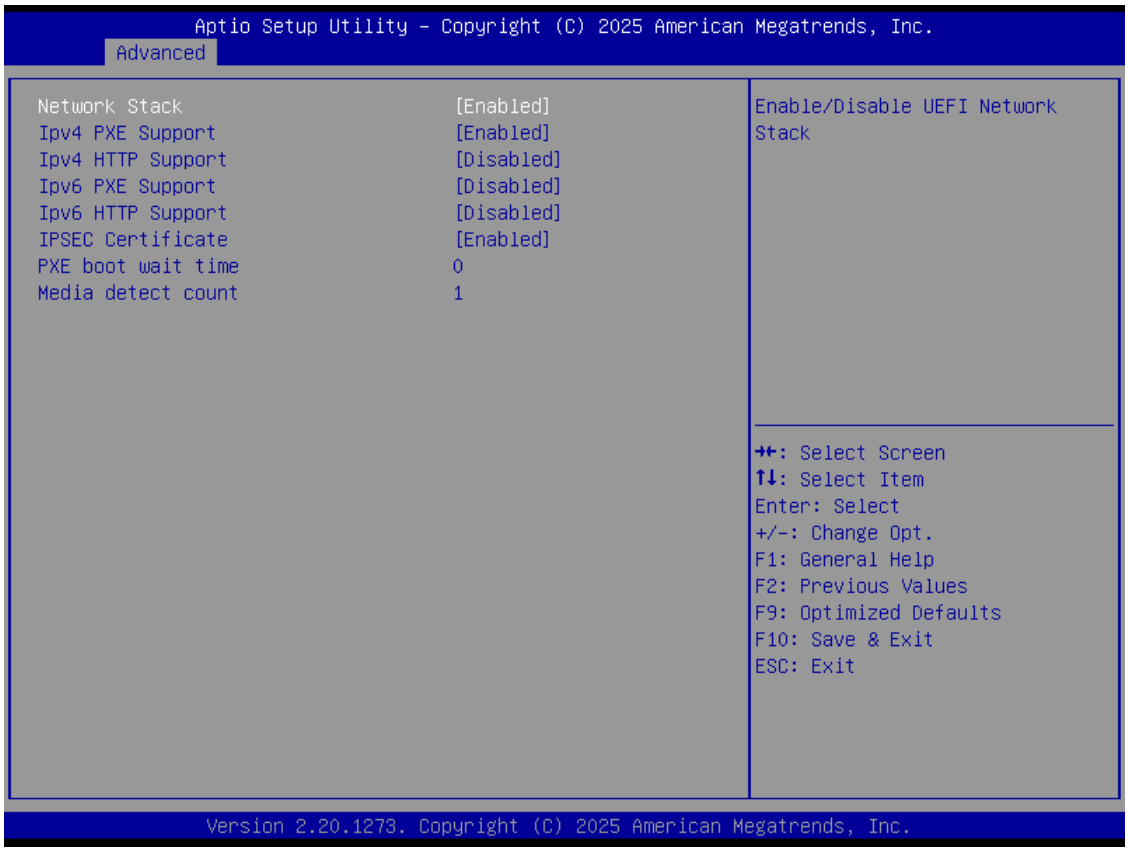
- By default, LVDS/eDP output is disabled.
- Once LVDS or eDP is enabled, the LVDS/eDP interface becomes the primary display output. All BIOS setup screens will be displayed only on the LVDS/eDP panel.
- Other display outputs (such as HDMI) will not display the BIOS interface while LVDS/eDP is active.
- Ensure that the LCD panel parameters are configured correctly before connecting the LVDS display.
- If incorrect panel parameters are selected and no display is shown, restore default settings by clearing the CMOS, then reconfigure the LVDS panel settings.

3.3.8 USB Configuration



- **Legacy USB Support:** Enable Legacy USB support. Disables legacy support if no USB devices are connected. Select enable will keep USB devices available under UEFI's support.
- **XHCI Hand-off:** A workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the USB XCHI driver.
- **USB Mass Storage Driver Support:** Enable(default) or disable USB Mass Storage Driver Support.
- **USB transfer time-out:** Time-out value for control, bulk, and interrupt transfers, default time:20 second.
- **Device reset time-out:** USB mass storage device starts unit command time-out, default time:20 second.
- **Device Power-up Delay:** Maximum time the device will take before it properly reports itself to the host controller.

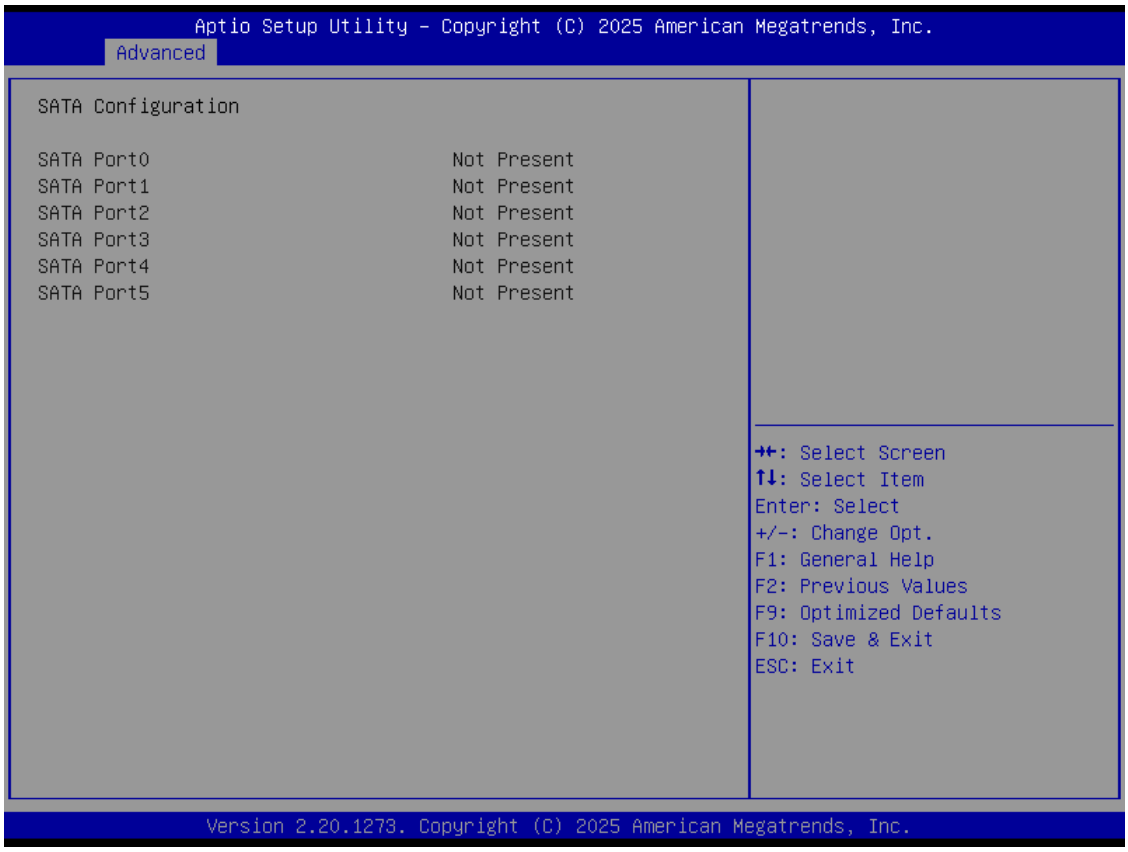
3.3.9 Network Stack Configuration



The Network Stack controls UEFI network boot (PXE/HTTP) and is disabled by default.

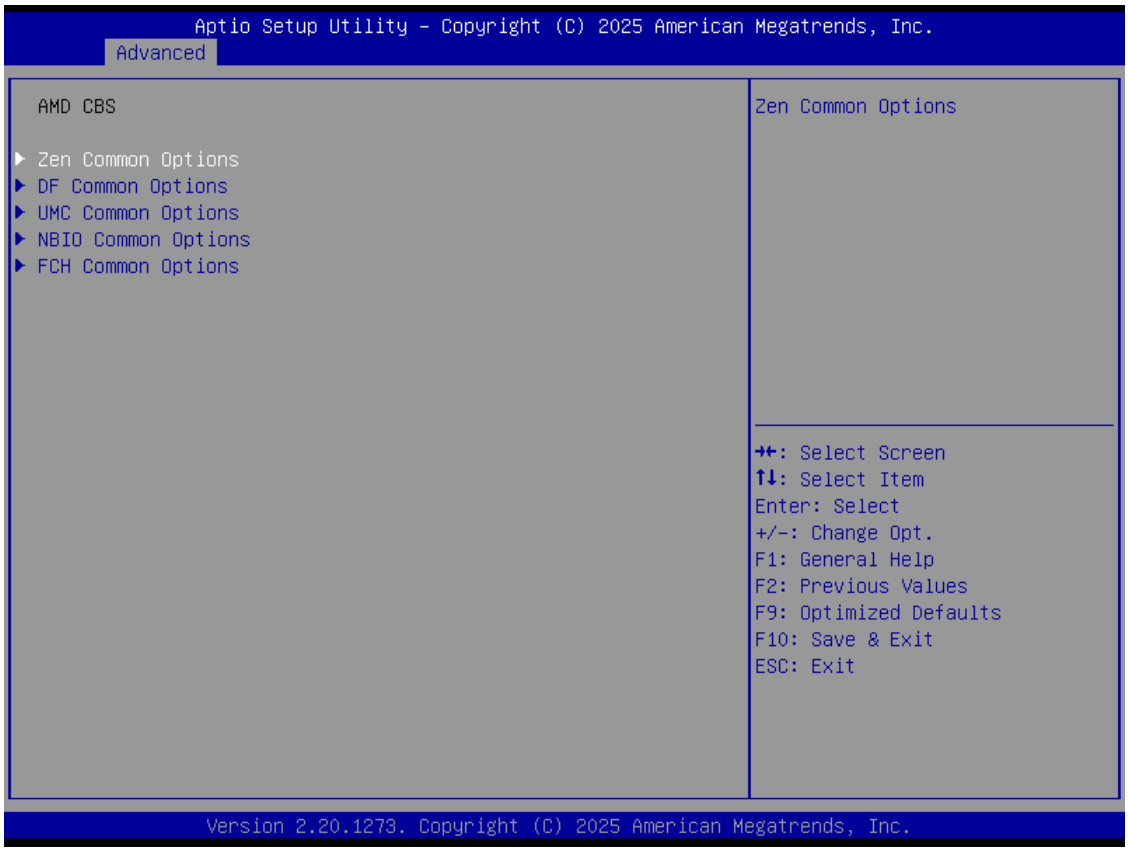
- **IPv4 PXE Support:** PXE boot over IPv4
- **IPv4 HTTP Support:** HTTP boot over IPv4
- **IPv6 PXE Support:** PXE boot over IPv6
- **IPv6 HTTP Support:** HTTP boot over IPv6
- **PXE Boot Wait Time:** Timeout delay for PXE boot
- **Media Detect Count:** Retry count for network device detection

3.3.10 SATA Configuration



The capacity and model of the storage device will be displayed under the option after the SATA protocol storage has been installed.

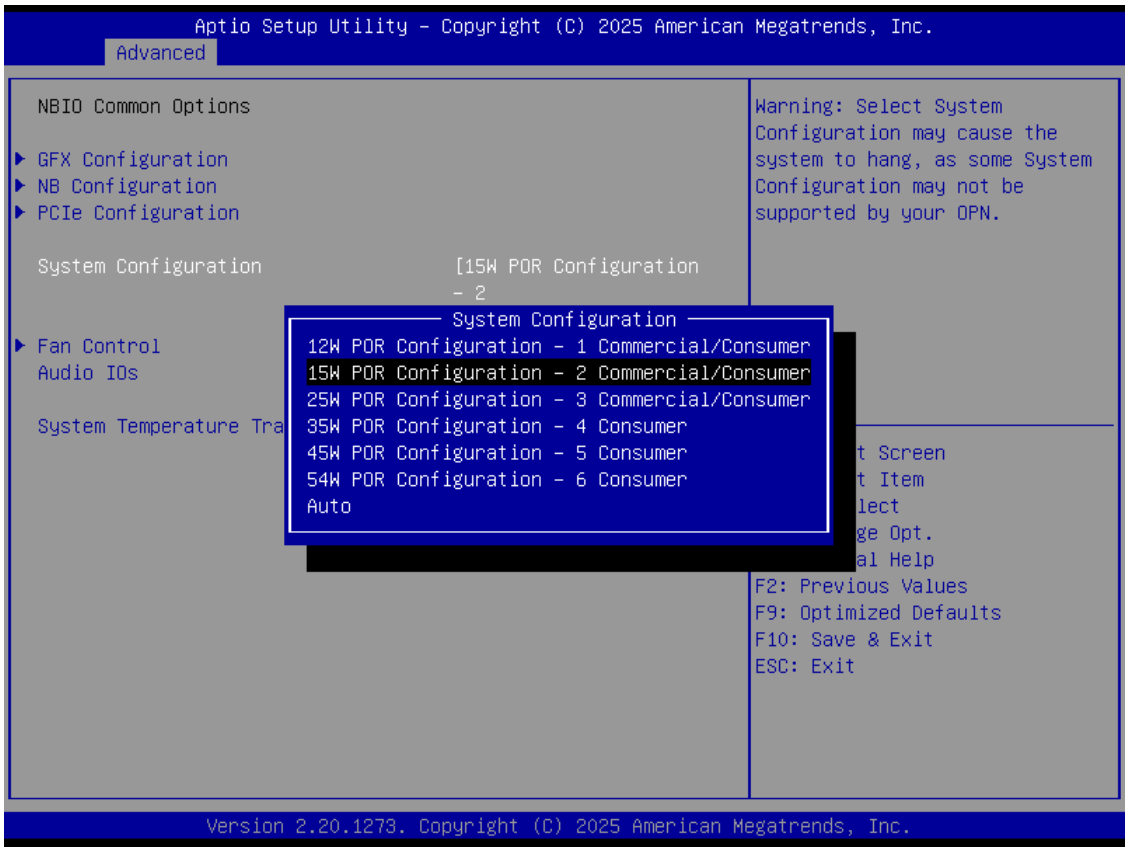
3.3.11 AMD CBS



The AMD CBS (Common BIOS Settings) menu provides access to advanced AMD platform configuration options.

- **Zen Common Options:** CPU configuration options
- **DF Common Options:** Data Fabric configuration options
- **UMC Common Options**: Unified Memory Controller options
- **NBIO Common Options:** Northbridge I/O options
- **FCH Common Options:** Fusion Controller Hub options

3.3.12 NBIO Common Options



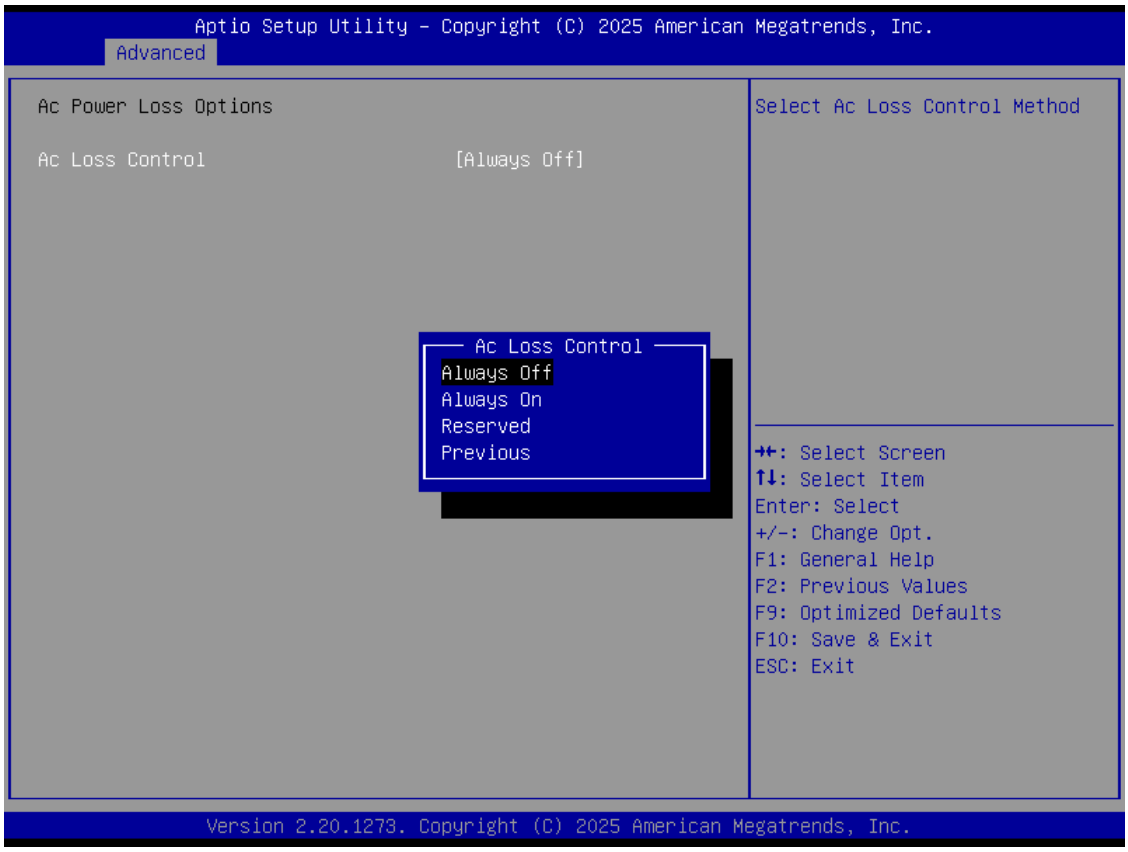
The NBIO (North Bridge I/O) Common Options menu provides configuration options for I/O, graphics, power management, and platform-related features.

Advanced > AMD CBS > NBIO Common Options>System Conifiguration

- CPU TDP Configuration: Allows configuration of the CPU TDP upper limit according to system thermal design.
  Default: 15 W
  Options: 12 W / 15 W / 25 W (availability depends on thermal configuration)

Note: The AMD Ryzen™ Embedded R2314 processor is designed for industrial control applications. Most third-party detection or monitoring utilities currently available on the market are consumer-grade tools and have not been fully adapted to accurately support this processor. As a result, power consumption readings reported by such software may be inaccurate. **For accurate power data, refer to the AMD official diagnostic tool AMD_SystemDeck_Tool (Windows) and check the values displayed under the PM tab.** In internal testing, when the BIOS TDP setting is configured to 15 W, the CPU reports approximately 6 W under stable load conditions. The actual power consumption is expected to be approximately 12–15 W, depending on workload and operating conditions.

3.3.13 FCH Common Options



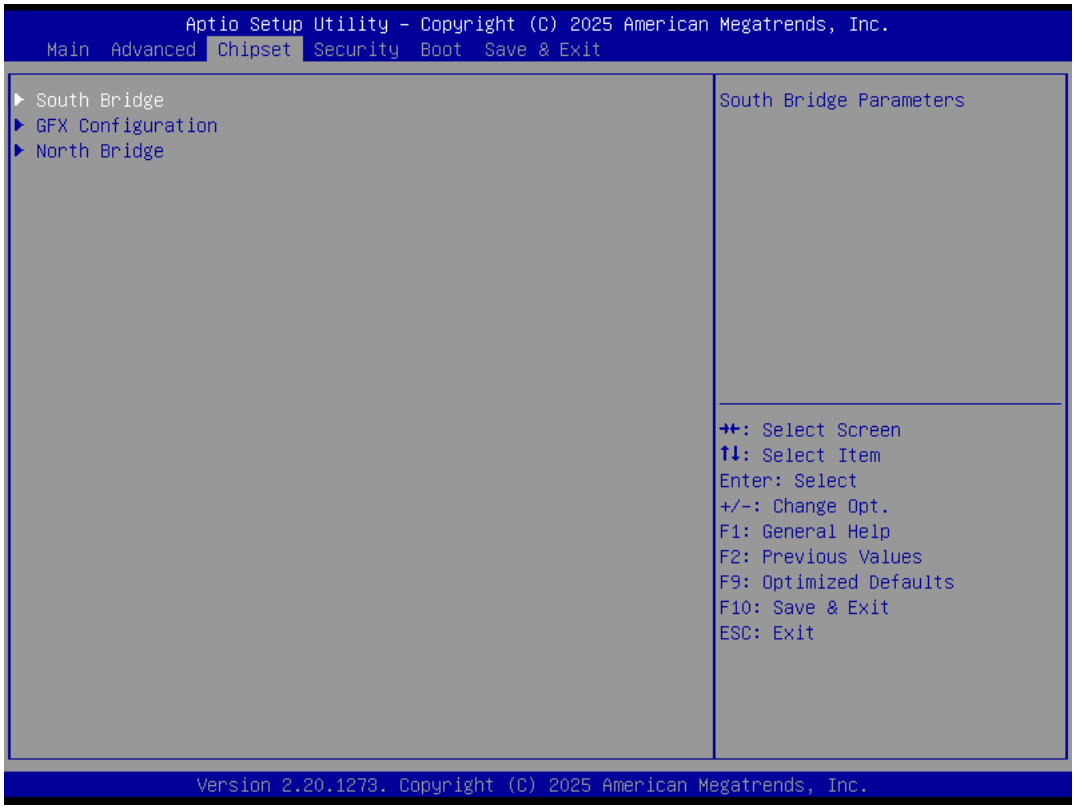
The FCH Common Options configure chipset-level power management and ACPI-related behavior, including system power-on behavior after AC power restoration.

Advanced > AMD CBS > FCH Common Options > AC Loss Control

AC Power Loss Options: Controls system behavior after AC power is restored.

- **Always Off (Default):** The system remains powered off when AC power is restored.
- **Always On:** The system automatically powers on when AC power is restored.
- **Reserved/Previous:** The system remains off after a normal shutdown. If AC power is lost unexpectedly, the system restores its previous power state when power is recovered**.**

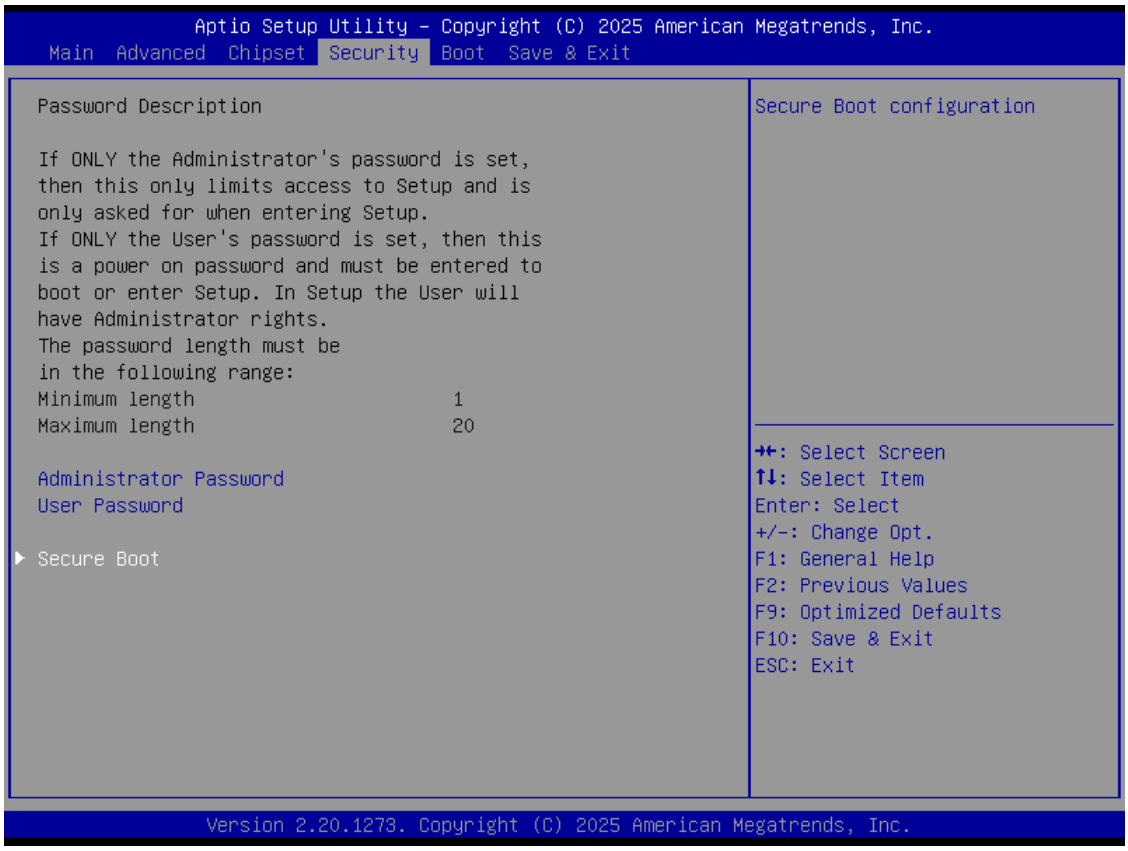
3.4 Chipset



Chipset

- **South Bridge:** Displays chipset-related configuration options for southbridge functions.
- **GFX Configuration (Not Supported):** Configures integrated graphics–related parameters, including display output behavior and graphics memory settings.
- **North Bridge:** Displays chipset-related configuration options for northbridge functions.

3.5 Security

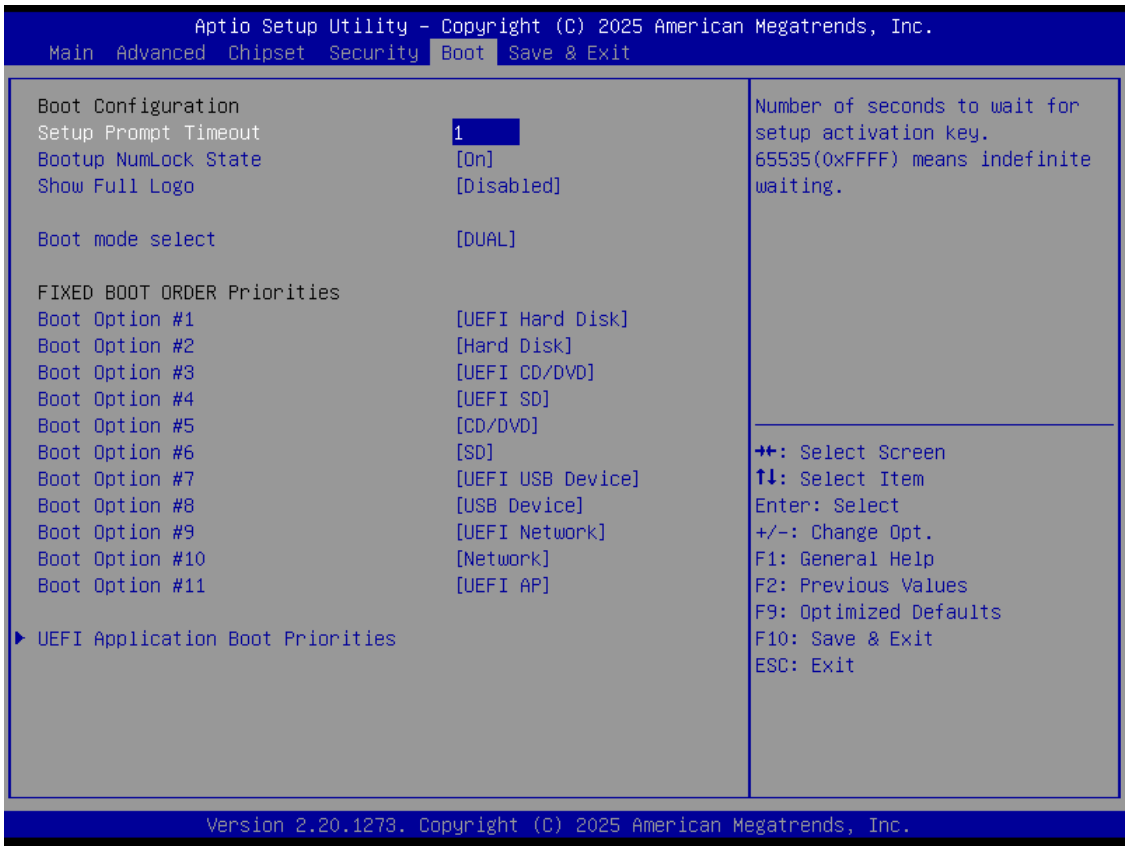


Administrator Password: Set the Administrator Password.

User Password: Set User Password.

Secure Boot: Configures Secure Boot settings.

3.6 BOOT



Setup Prompt Timeout:

Number of seconds that the firmware will wait before initiating the original default boot selection. A value of 0 indicates that the default boot selection is to be initiated immediately on boot. A value of 65535(0xFFFF) indicates that firmware will wait for user input before booting. This means the default boot selection is not automatically started by the firmware.

Bootup NumLock State:

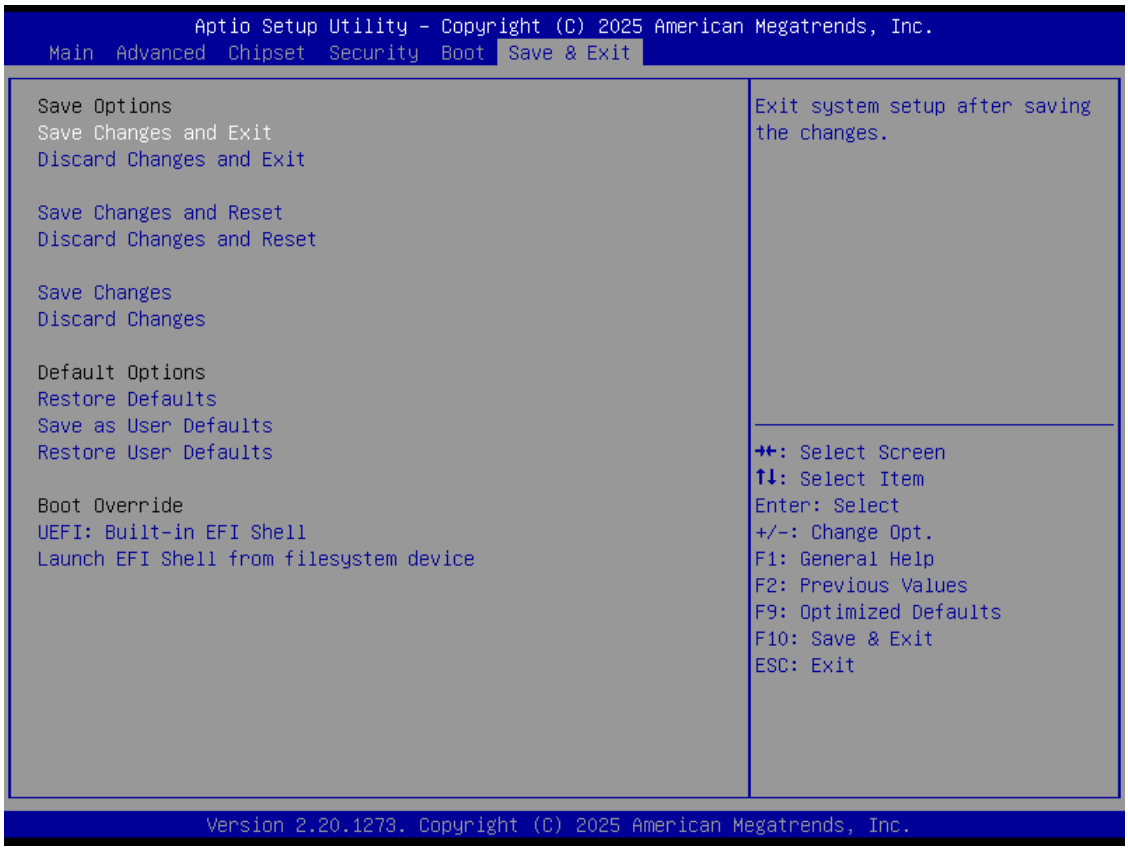
Select the keyboard NumLock State. This option specifies the state of the keyboard NumLock function after the system starts. When set to On (default), the numeric keypad is enabled for number entry immediately after startup. When set to Off, the numeric keypad operates in cursor control mode during startup.

Show Full Logo: Enabled/Disabled Displays customized boot logo.

Boot Option #1~#11: Set the system boot order from Number 1 to Number 11.

UEFI Application boot Priorities: UEFI application boot priority.

3.7 Save & Exit



Save Changes and Exit: Exit the system setup after saving the changes and continue to start the computer.

Discard Changes and Exit: Exit the system setup without saving any changes and continue to start the computer.

Save Changes and Reset: Reset the system after saving the changes.

Discard changes and Reset: Reset the system without saving any changes.

Save Changes: Save changes done so far to any of the options.

Discard Changes: Discard changes done so far to any of the options.

Restore Defaults: Restore/load default values for all the options.

Save as User Defaults: Save the changes done so far as the user defaults.

Restore User Defaults: Restore the user defaults to all the options.

Boot Override: Boot device selection can override your boot priority. Select the specified boot device such as SATA, USB Flash Disk, EFI Shell, PXE, etc., and boot directly. Or press F11 boot by selecting the specified boot device.

- **UEFI: Built-in EFI Shell**: Launches the built-in UEFI EFI Shell.
- **Launch EFI Shell From Filesystem Device**: Launches the EFI Shell from a filesystem device.

Appendix

GPIO Setting

Accessing GPIO70:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x01); //Bit0=1 set as output，bit0=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x01); // When set as output, Bit0 of I/O address 0xA06 = 1 outputs high level, Bit0 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit0=1 Set as output，bit0=0 Set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); //When set as input, Bit0 of I/O address 0xA06 reflects the read state.

Accessing GPIO71:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x02); // Bit1=1 set as output， bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x02); // When set as output, Bit1 of I/O address 0xA06 = 1 outputs high level, Bit1 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); // Bit0=1 set as output， bit1=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit1 of I/O address 0xA06 reflects the read state.

Accessing GPIO72:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x04);    //Bit2=1 set as output，bit2=0 set as input
WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x04); // When set as output, Bit2 of I/O address 0xA06 = 1 outputs high level, Bit2 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit2=1 set as output，bit2=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit2 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO73:

Example: Accessing via IO

Set as output：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x08); //Bit3=1 set as output，bit3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x08); // When set as output, Bit3 of I/O address 0xA06 = 1 outputs high level, Bit3 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit3=1 set as output，bi3=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit3 of I/O address 0xA06 reflects the read state.

Accessing GPIO74:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x10); //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x10); // When set as output, Bit4 of I/O address 0xA06 = 1 outputs high level, Bit4 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit4=1 set as output，bit4=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit4 of I/O address 0xA06 reflects the read state.

Accessing GPIO75:

Example: Accessing via IO

Set as output:

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x20); //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x20); // When set as output, Bit5 of I/O address 0xA06 = 1 outputs high level, Bit5 = 0 outputs low level

Set as input：

WriteIo8(0x2e, 0x87);

WriteIo8e(0x2e, 0x01);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);

WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);

WriteIo8 (0x2f, 0x00); //Bit5=1 set as output，bit5=0 set as input

WriteIo8 (0x2e, 0x02);

WriteIo8 (0x2f, 0x02);

temp = ReadIo8 (0xA06); // When set as input, Bit5 of I/O address 0xA06 reflects the read state.

Accessing GPIO76:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x40);    //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x40); // When set as output, Bit6 of I/O address 0xA06 = 1 outputs high level, Bit6 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit6=1 set as output，bit6=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit6 of I/O address 0xA06 reflects the read state.
```

Accessing GPIO77:

Example: Accessing via IO

Set as output:

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x80);    //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

WriteIo8 (0xA06, 0x80); // When set as output, Bit7 of I/O address 0xA06 = 1 outputs high level, Bit7 = 0 outputs low level
```

Set as input：

```
WriteIo8(0x2e, 0x87);
WriteIo8e(0x2e, 0x01);
WriteIo8 (0x2e, 0x55);
WriteIo8 (0x2e, 0x55);

WriteIo8 (0x2e, 0x07);
WriteIo8 (0x2f, 0x07);

WriteIo8 (0x2e, 0xce);
WriteIo8 (0x2f, 0x00);    //Bit7=1 set as output，bit7=0 set as input

WriteIo8 (0x2e, 0x02);
WriteIo8 (0x2f, 0x02);

temp =    ReadIo8 (0xA06); // When set as input, Bit7 of I/O address 0xA06 reflects the read state.
```